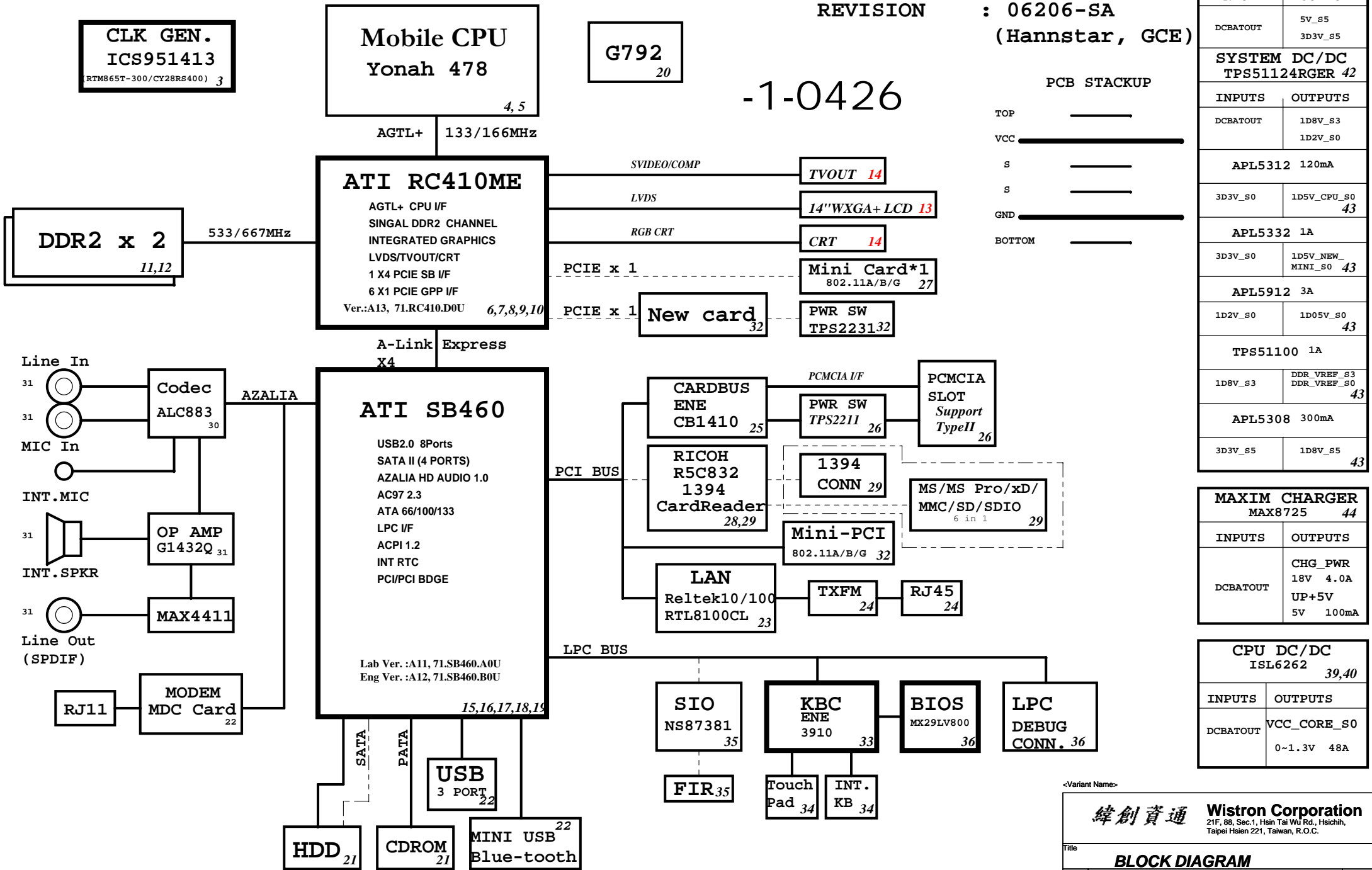
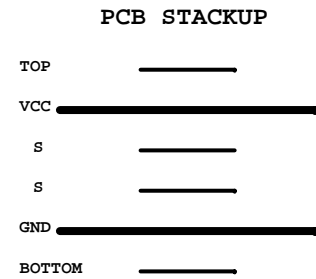


Garda-5 Block Diagram

Project code: 91.4Q201.001
 PCB P/N : 55.4Q201.XXX
 REVISION : 06206-SA
 (Hannstar, GCE)



-1-0426



SYSTEM DC/DC TPS51120 41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
SYSTEM DC/DC TPS51124RGER 42	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D2V_S0
APL5312 120mA	
3D3V_S0	1D5V_CPU_S0 43
APL5332 1A	
3D3V_S0	1D5V_NEW_MINI_S0 43
APL5912 3A	
1D2V_S0	1D05V_S0 43
TPS51100 1A	
1D8V_S3	DDR_VREF_S3 DDR_VREF_S0 43
APL5308 300mA	
3D3V_S5	1D8V_S5 43

MAXIM CHARGER MAX8725 44	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 1.8V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 39,40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 48A

<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

Size A3 Document Number **Garda-5** Rev **-1**

Date: Wednesday, April 26, 2006 Sheet 1 of 46

USB	
Pair	Device
0	USB1
1	BT
2	USB2
3	NEW C
4	USB3
5	CCD
6	MINIC1
7	NC

PCI_CLK0 PCMC
PCI_CLK1 IEEE1394
PCI_CLK2 LAN
PCI_CLK3 MINI
PCI_CLK4 KBC
PCI_CLK5 FWB
PCI_CLK6 SIO
PCI_CLK7 SPDIFOUT

PCI ROUTING TABLE			
DEVICE	IDSEL	IRQ(Default)	REQ# / GNT#
MiniPCI	AD22	H	REQ#1/ GNT#1
R5C832	AD20	F: 1394 H: 6 in 1	REQ#3/ GNT#3
LAN(RTL8100CL)	AD17	E	REQ#2/ GNT#2
CARDBUS CB1410	AD16	G	REQ#0 / GNT#0
USB UHCI	AD29	A, B, C, D	
USB 2.0 EHCI	AD29	A	
DMI-to-PCI AC97 Modem AC97 Audio	AD30	B A	REQ#1 / GNT#1
LPC Bridge IDE SATA SMBus	AD31	A B B	
PCI Express	AD28	A, B, C, D	
Azalia Controller	AD27	A	

History

2006/04/26 (-1 Modify)
 1. page 27, change R8/R226 to 100 ohm due to power/email to dark.
 2. page 15, change C286/C287 from 18pf to 15pf due to frequency shift(from -6.7 to 4ppm).
 3. page 23, change C295/C294 from 15p to 12p due to frequency shift(from -23.3 to 7.9ppm).
 4. EMI Solution for USB/MDC
 a. Change L23, L24, L31, L32 to "69.10084.071".
 b. del R353,R354,R356,R360,R445,R446.
 c. Change L1, L2 to "68.00331.011".
 5. Page 44, change C12/C14 to 78.10699.43L due to 78.10699.42L Obsoleted.

2006/04/13 (-1 Modify)
 1. Page 31, R447/R448 tp 33ohm.
 2. Page 45, Add D4:83.P4SSM.0AM.
 3. Page 44, Change C321 from 78.10492.4BL to 78.10224.2BL(1000P, 50V, K0603).
 4. Page 23, change R209 from 5.6K to 5.37K.
 5. Page 24, change XF1 from 68.68161.30A to 68.01201.30A.
 6. Page 46, Mini card stand-off(銅柱) need to be changed from 34.4P401.001 to 34.4A907.001.
 7. change 84.27002.L04 to 84.27002.F31.

2006/04/10 (-1 Modify)
 1. Page 8, add "LVDS DIGON" solution from ATI PA note.
 2. Page 31, Add R to GND and serial R for U60 pin13/15.

2006/04/03 (SB Modify)
 1. Page 40, Dummy C593.
 2. Page 44, Del C32.
 3. Page 41, DCBATOUT 51120 change to DCBATOUT (Del G4,G5,G6,G7,G8)
 4. Page 4/5, update CPU symbol.
 5. Page 15, Change X5 to same as X1 due to ME high limit issue, Cap. the same as X1 but should fine-tune.
 6. Page 39/41/42, change "GAP-CLOSE-PWR" to 0 ohm PAD due to layout concern.

2006/03/31 (SB Modify)
 1. Page 3, change R139 to bead and C211 to 2.2u for CRT Jitter.
 2. Page 6, change R105 from 1.8K to 4.7K.
 3. Page 8, change C165 to 2.2u for ATI recommend.
 4. Page 8, SIV EDID_CLK/DAT issue, change RN53 to 4.7K.
 5. Page 14, SIV RBG fail:
 6. Page 15,
 a. PCIRST1#(1394) shoulder: Add 33 ohm @ SB.
 b. PLT_RST1# overshoot : change R144 to 33ohm & R141 to 100P.
 c. Add 0ohm for RTC power for ATI recommend.
 7. Page 40 , add 10U Cap.
 8. Page 13/27, change Green LED4/LED5/LED1 to 83.00190.L70.
 (manual change yellow LED6/LED3/LED8/LED2 to 83.00190.S70).
 9. EMI request:
 a. Page 13, USB PP5,USB PN5 add COMMON CHOKE.
 b. EC28,EC34,C208 add 0.1uCap.
 c. CLK48_ICH(near CLK GEN.),SB_CLK33_FWH(near R177) add 20p Cap..

2006/03/28 (SB Modify)
 1. Page 14, change Q15/Q14 to 2N7002 for SIV CRT SMBus bug.
 2. Page 15, Change C248/C261/C264/C263/C252 from 78.10491.4FL to 78.10523.5F1,
 and C262 from 78.10693.41L to 78.10623.51L.
 3. Page 8, Add "LCDVDD_ON" PL 100K.
 4. Page 41, change U7 to A04406(84.04406.A37).
 5. Page 33, KBC GPIO09 for 1394.
 6. Page 33, add 1u Cap. for ENE ECRST# spec. 2ms.
 7. Page 31, add audio popo noise solution.
 8. Page 25, change C520 to 1U for "GBRST#".
 9. Page 28, change "GBUS_GRST#_1" timing.

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,.....

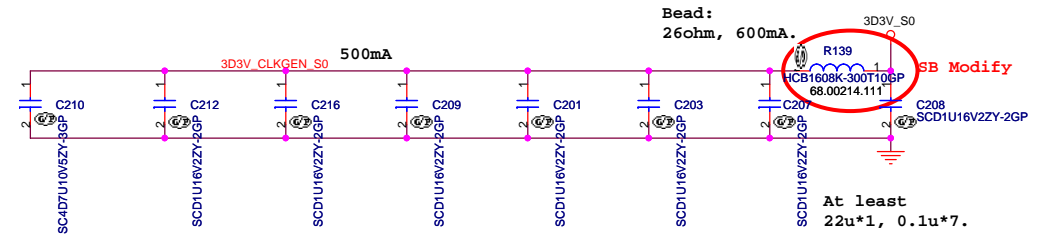
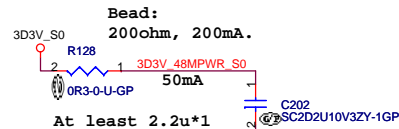
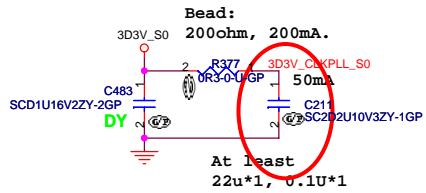
CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
 Capacitor type + value + rating + size + tolerance + material
 SCD1U10V2MX-1
 SC=> SMT Ceremic, TC=> POS cap or SP cap
 D1U => 0.1uF
 10V => the voltage rating is 10V
 2=> 0402, 3=>0603, 5=>0805
 M=>tolerance J, K, M, Z
 X=> X7R/X5R, Y=> Y5V
 -1 => symbol version, nonsense to EE characteristic

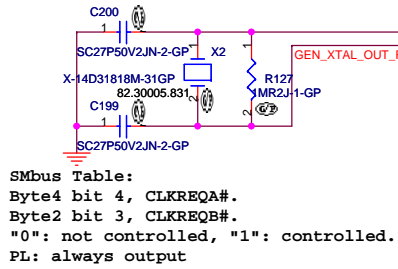
<Variant Name>

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Reference			
Title	Document Number		Rev
	Garda-5		-1
Date:	Wednesday, April 26, 2006	Sheet	2 of 46

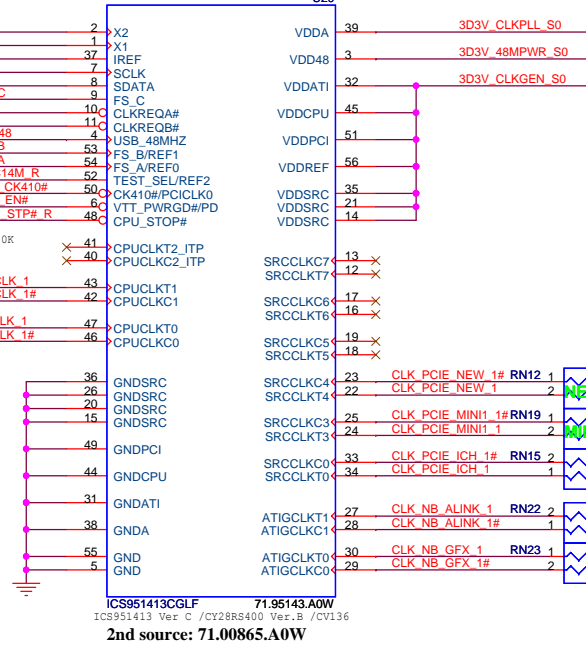
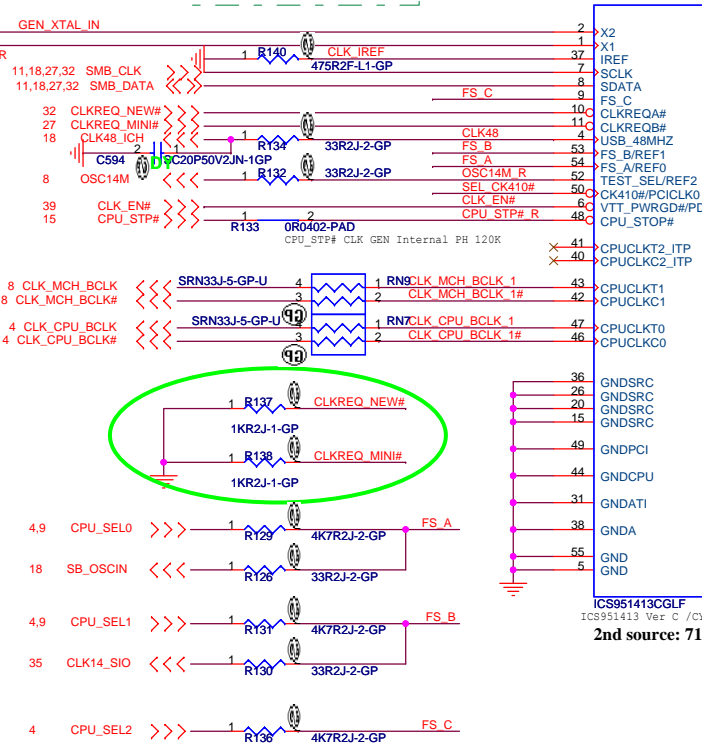


$$I_{oh} = 6 * I_{ref} (2.32mA)$$

$$V_{oh} = 0.7V @ 50 ohm$$



NB free-running:
 Byte5 bit5 = 0.



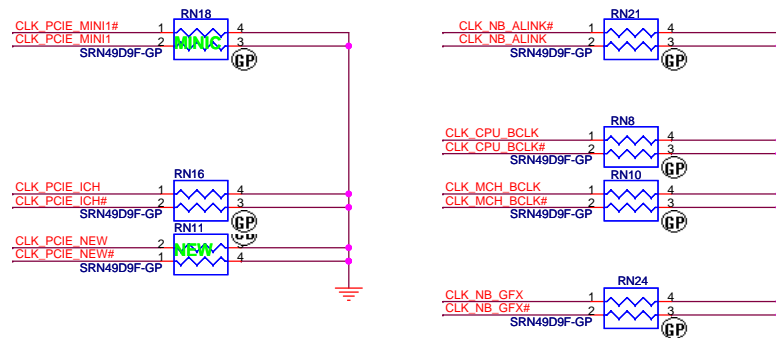
CK410# = 0, CK410 MODE

CK410# = 1, CK409 MODE

CLOCK FREQUENCY SELECT TABLE (MHz)

FSC	FSB	FSA	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	RESV	100	33	14.31

For Yonah Cerlon-M
 For Yonah



<Variant Name>

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Title: **Clock Generator -ICS951413**

Size A3 Document Number **Garda-5** Rev **SB**

Date: Wednesday, April 26, 2006 Sheet 3 of 46

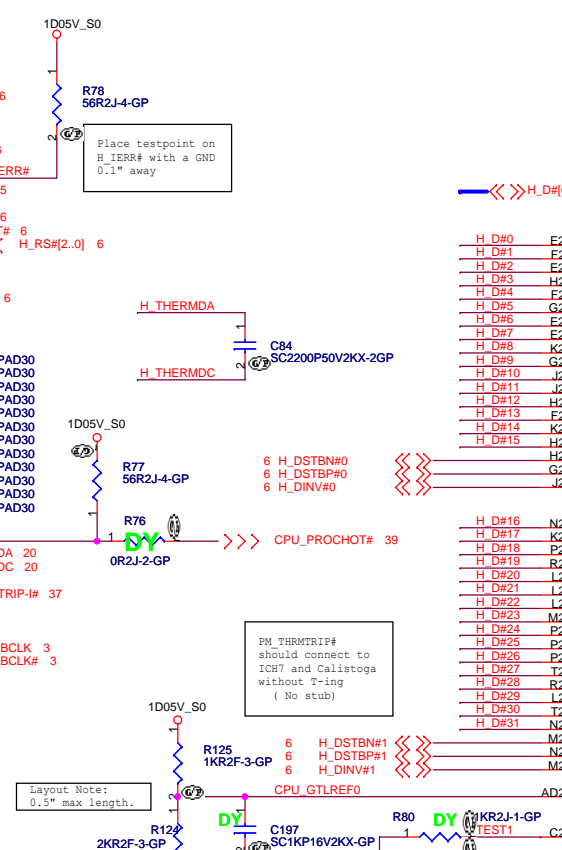
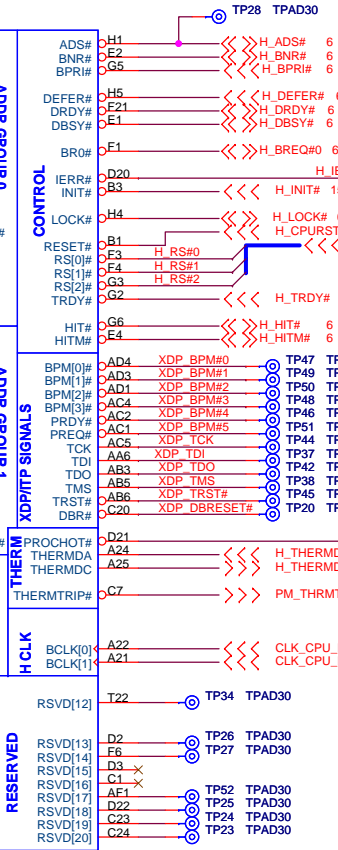
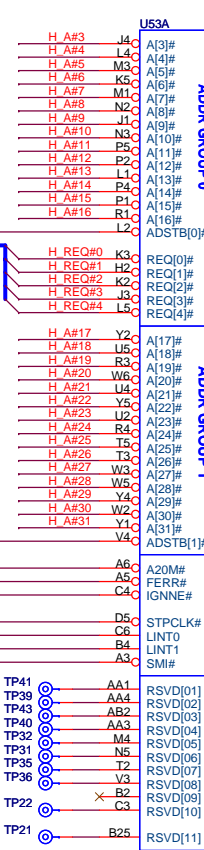
6 H_A#[31..3]

6 H_ADSTB#0
6 H_REQ#[4..0]

6 H_ADSTB#1

15 H_A20M#
15 H_FERR#
15 H_IGNNE#

15 H_STPCLK#
15 H_INTR#
15 H_NMI#
15 H_SMI#



Layout Note:
0.5" max length.

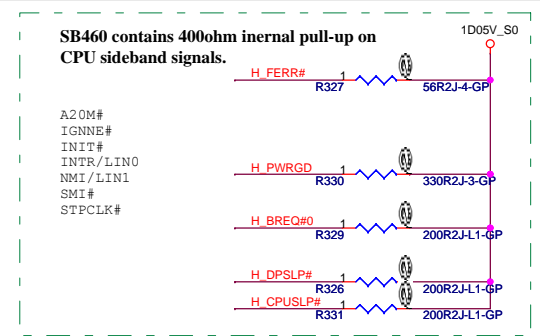
PM_THRMTRIP# should connect to ICH7 and Calistoga without T-ing (No stub)

CPU_GTLREF0

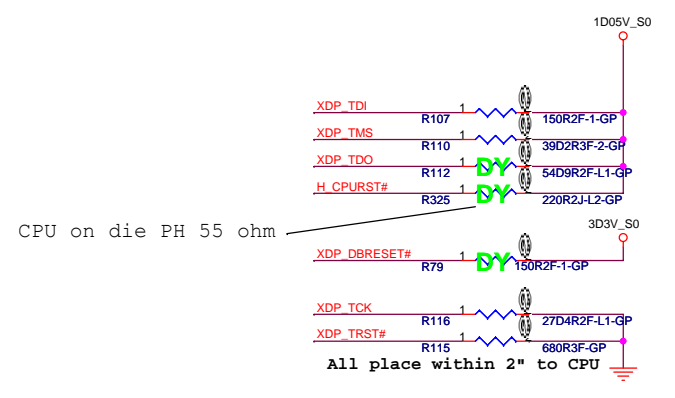
CPU_SEL0 3.9
CPU_SEL1 3.9
CPU_SEL2 3

H_DPRSLP#

PM_DPRSLPVR 15.39



Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .



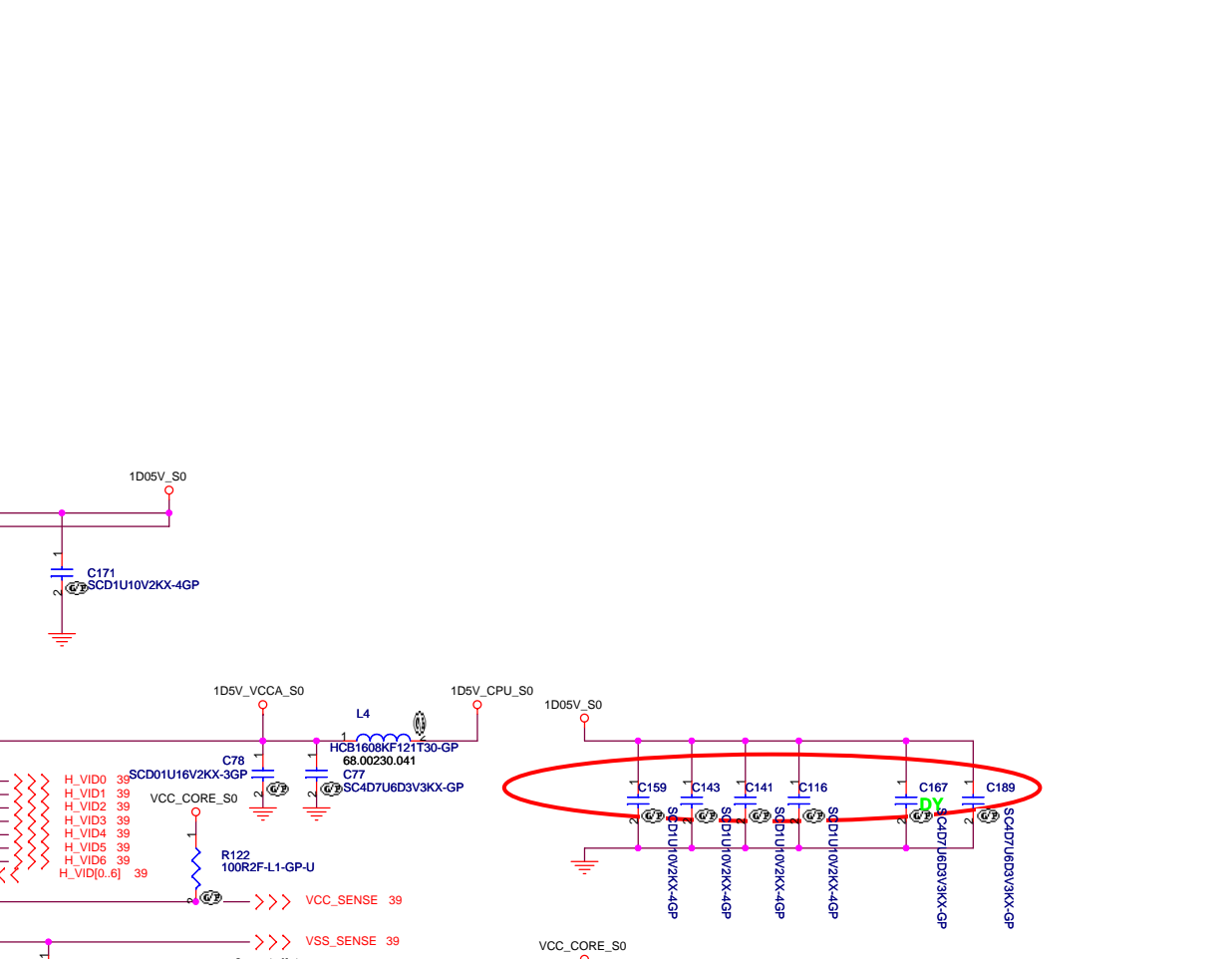
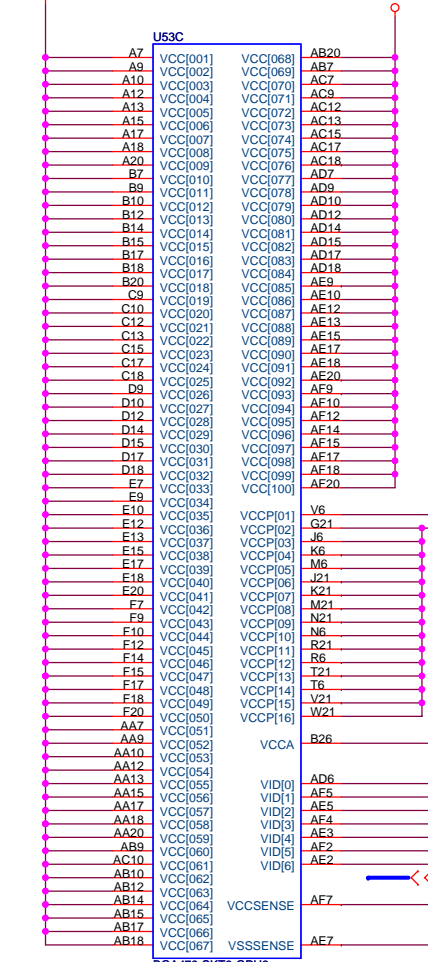
Wistron Corporation
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File: **CPU (1 of 2)**

Size: A3 Document Number: **Garda-5** Rev: **SA**

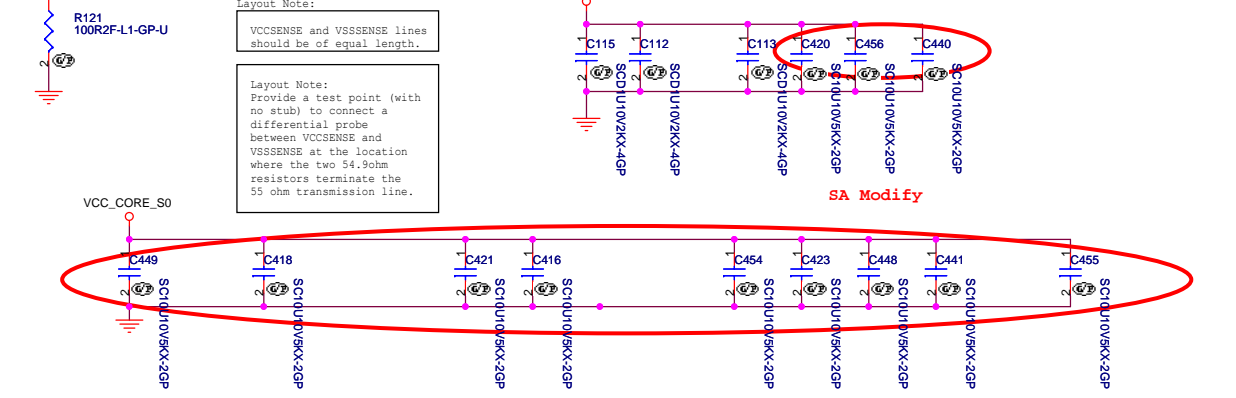
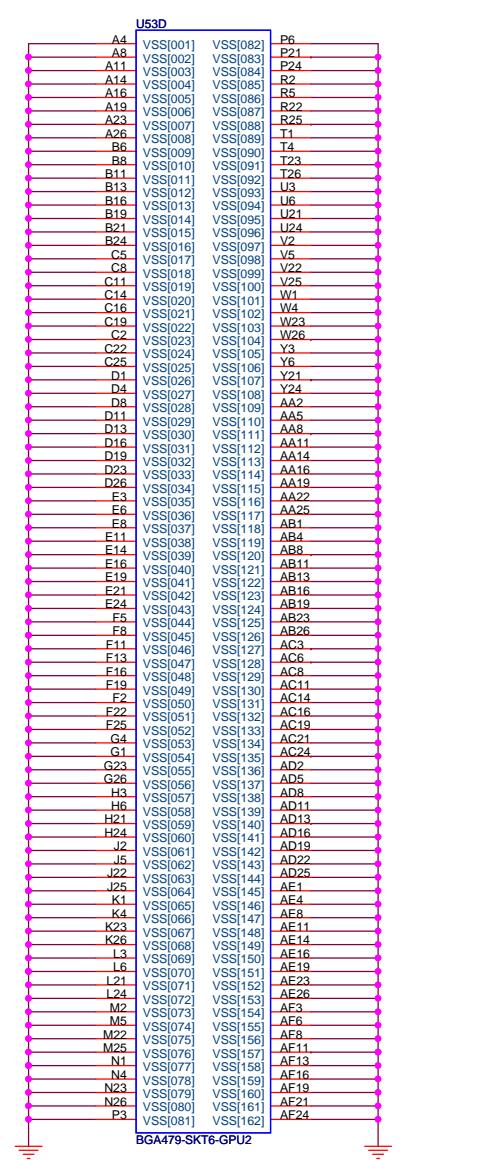
Date: Wednesday, April 26, 2006 Sheet 4 of 46

VCC_CORE_S0



Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

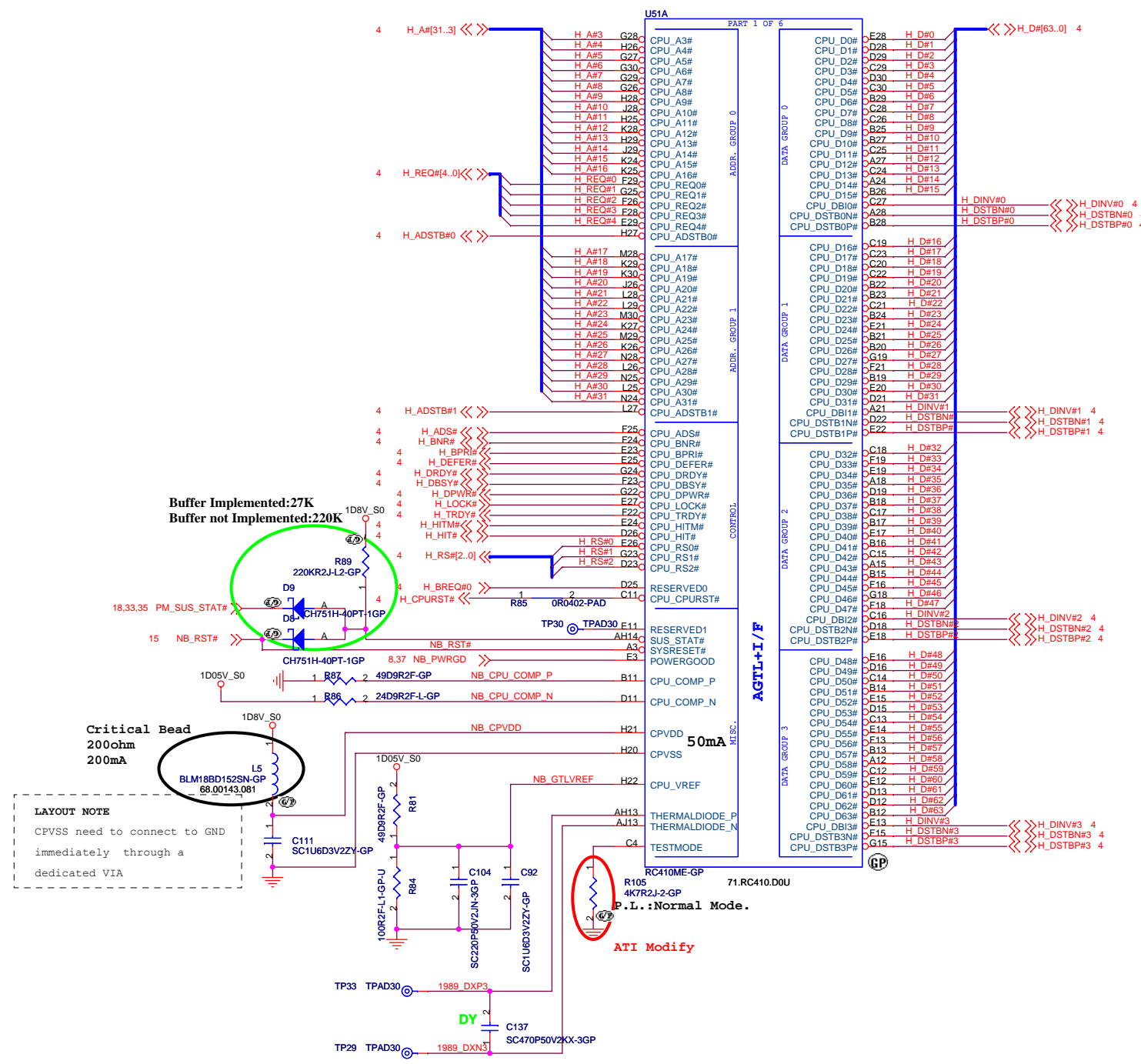


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Title: **CPU (2 of 2)**

Size A3 Document Number: **Garda-5** Rev: **SA**

Date: Wednesday, April 26, 2006 Sheet 5 of 46



Buffer Implemented:27K
Buffer not Implemented:220K

Critical Bead
200ohm
200mA

LAYOUT NOTE
CPVSS need to connect to GND immediately through a dedicated VIA

<Variant Name>

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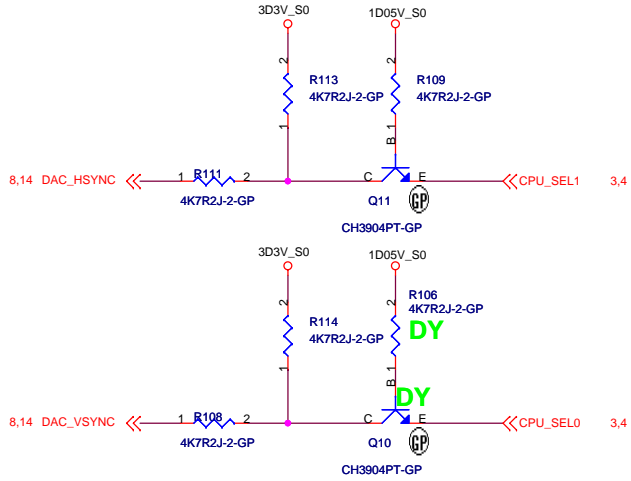
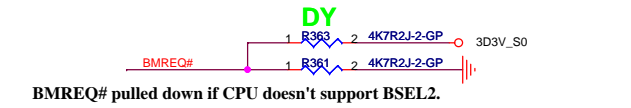
Title: **RC410ME (1 of 5) Host I/F**

Size A3 Document Number **Garda-5** Rev **SB**

Date: Wednesday, April 26, 2006 Sheet 6 of 46

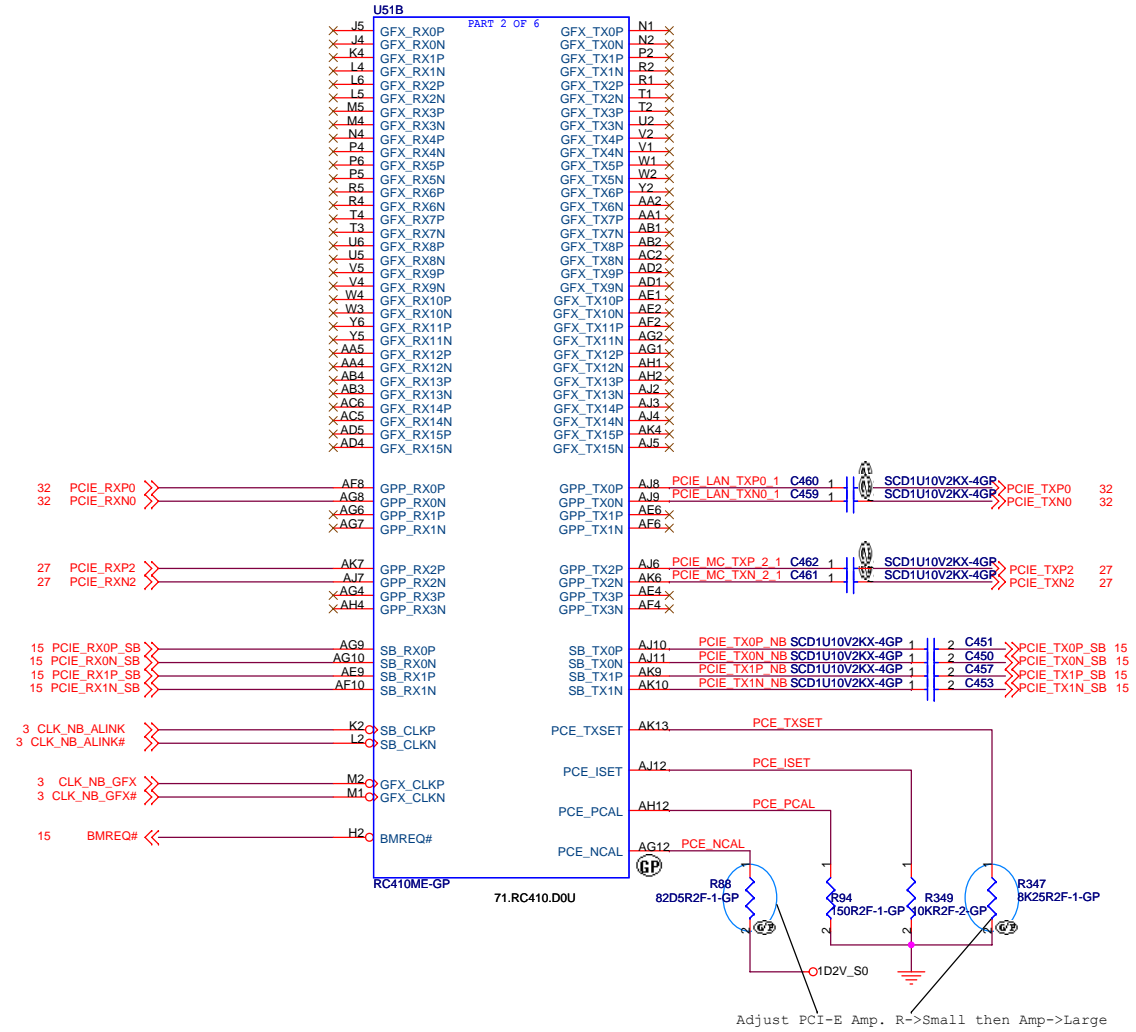
NB Strap pins

All pull-up and pull-down resistors are 4.7kohm.



Select the FSB SPEED

BMREQ#	HSYNC	VSYNC	Freq.
0	0	0	100MHZ
0	0	1	133MHZ
0	1	0	-----
0	1	1	166MHZ
1	0	0	100MHZ
1	0	1	100MHZ
1	1	0	-----
1	1	1	-----



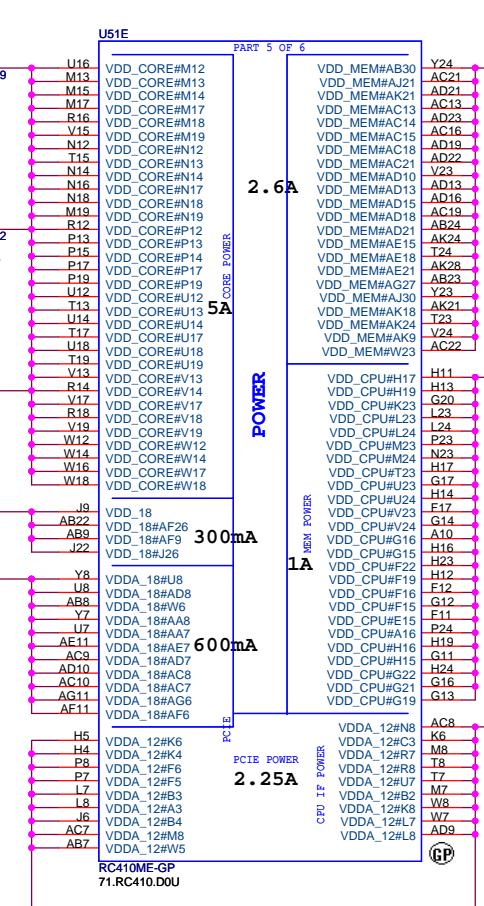
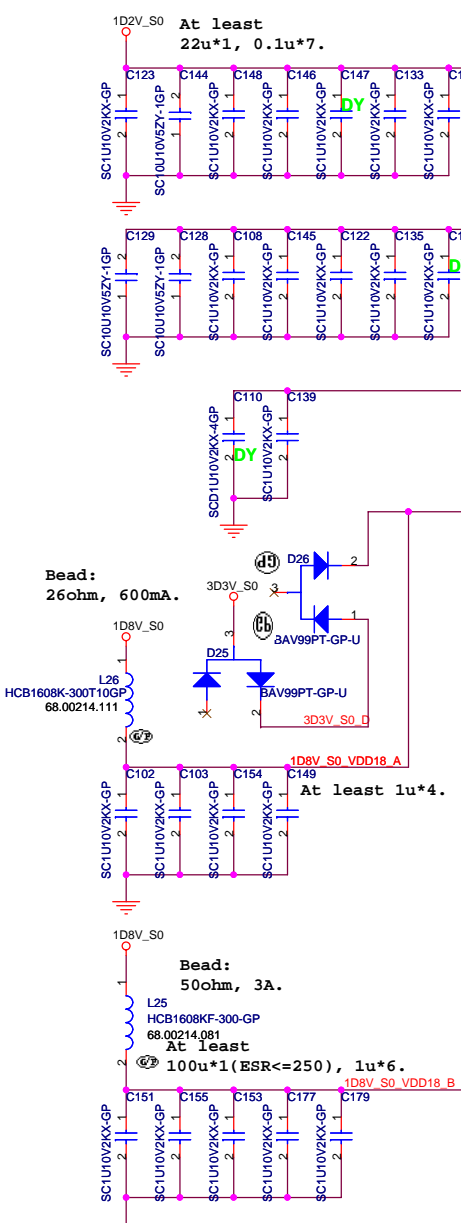
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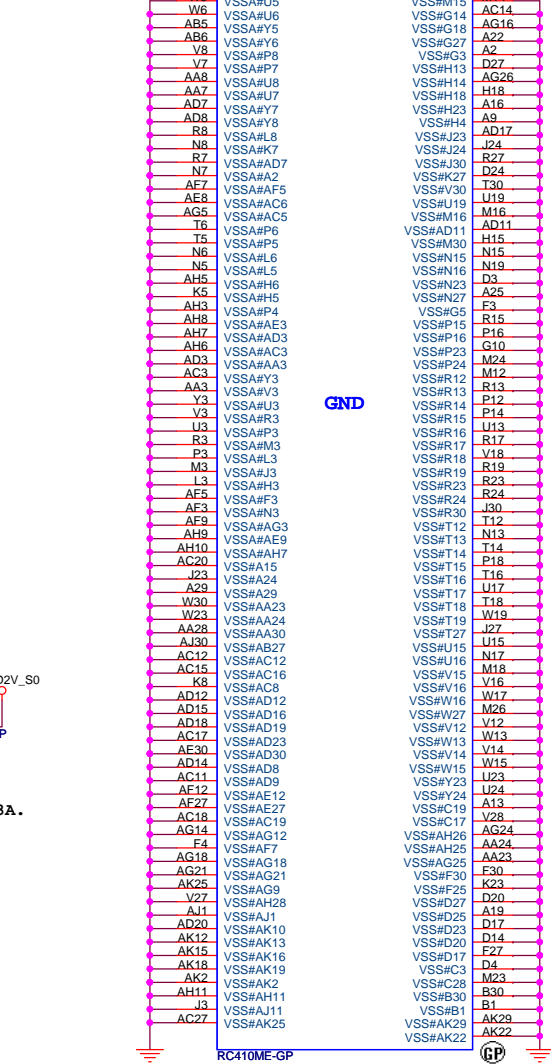
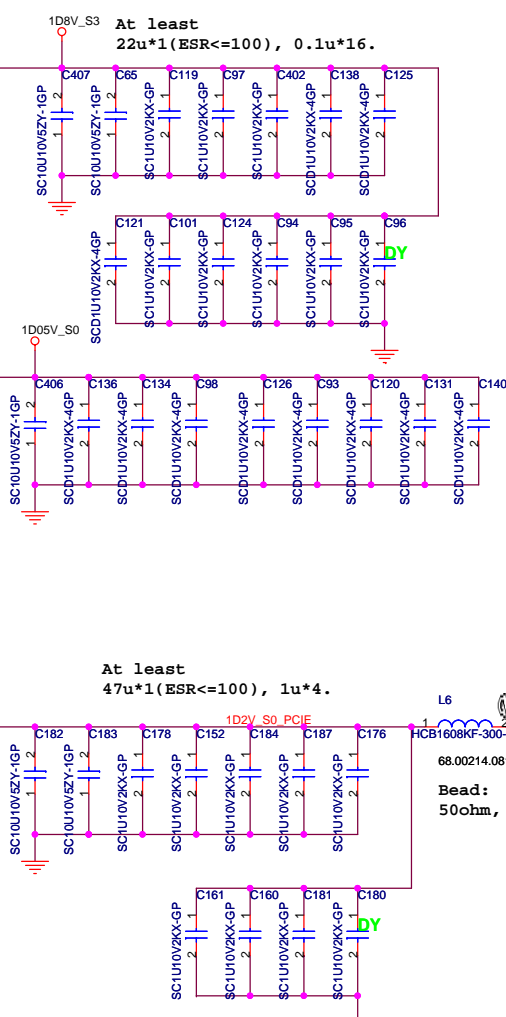
Title: **RC410ME (4 of 5) PCI-E & Strap**

Size: A3 Document Number: **Garda-5** Rev: **SA**

Date: Wednesday, April 26, 2006 Sheet 9 of 46



Supply	Signal group	Icc-max
1D2V_S0	VDD_CORE	5A
1D8V_S0	VDD_18	1.37A
1D2_S0	VDDA_12	2.25A
1D8V_S3	VDD_MEM	2.6A
1D05V_S0	VDD_CPU	1A

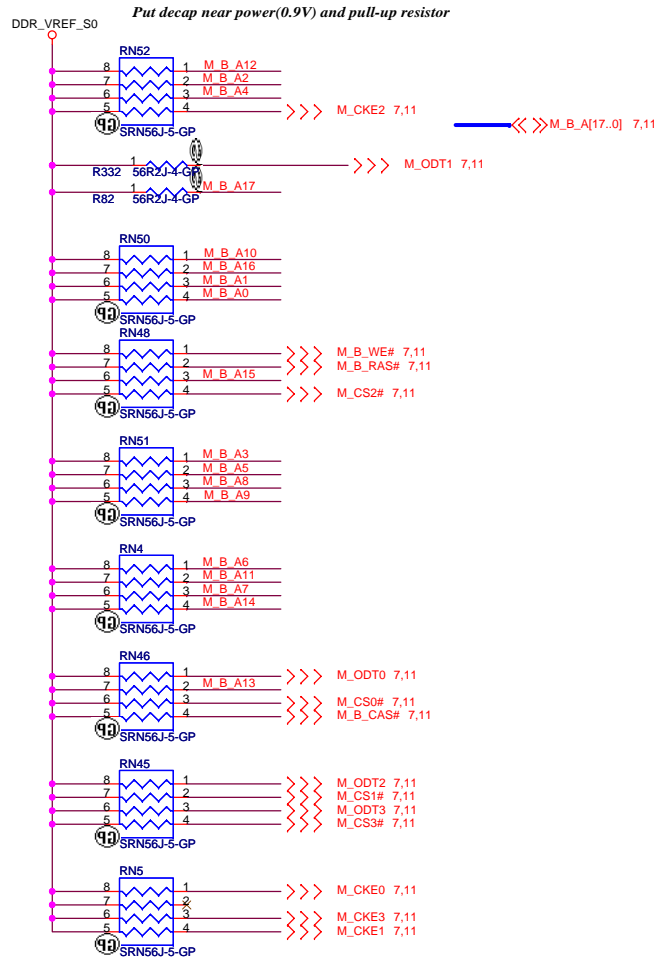


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 Taipei Hsien 221, Taiwan, R.O.C.

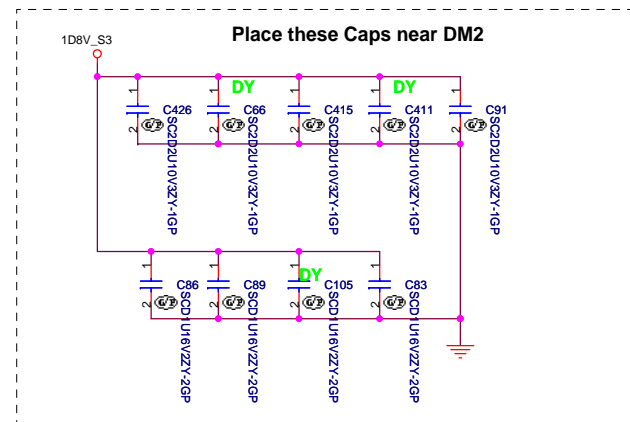
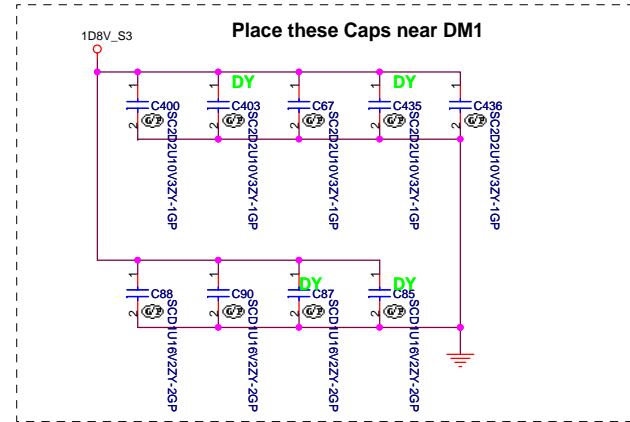
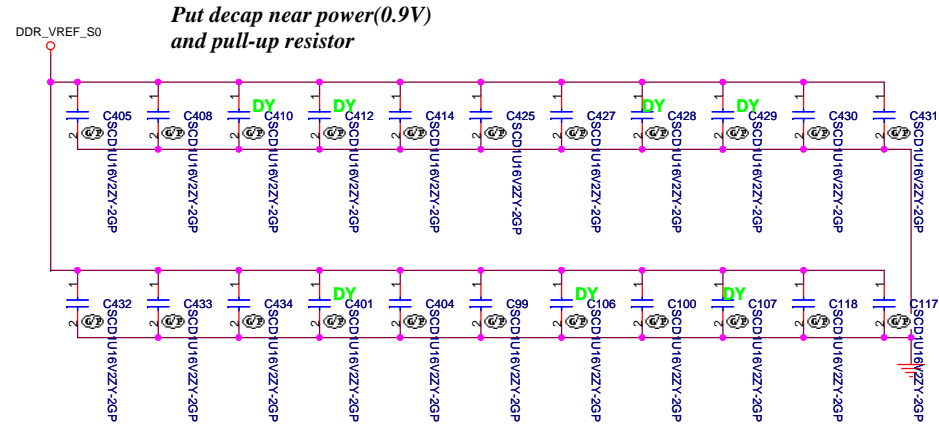
RC410ME (5 of 5) Power
Garda-5

Title: _____
 Size: A3 Document Number: _____ Rev: SA
 Date: Wednesday, April 26, 2006 Sheet 10 of 46

PARALLEL TERMINATION



Decoupling Capacitor



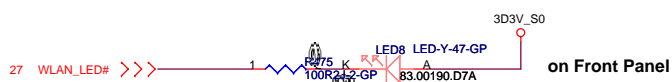
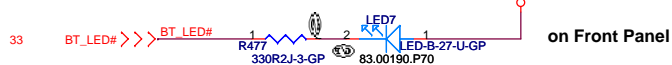
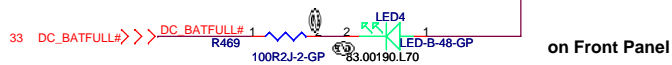
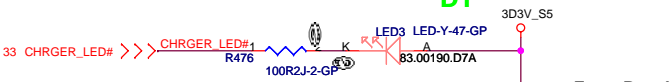
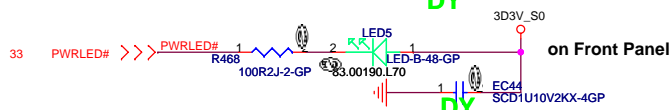
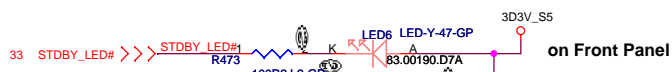
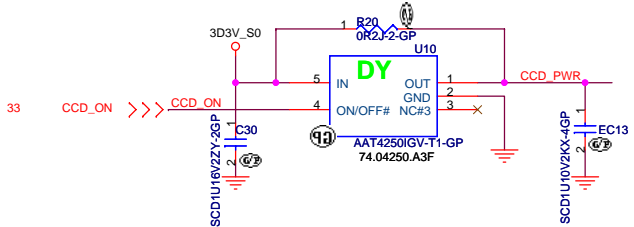
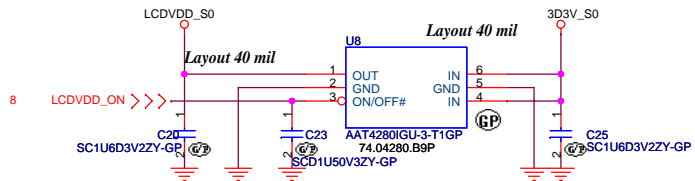
<Variant Name>

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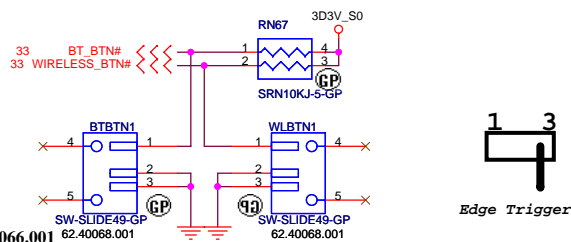
Title: **DDR2 Termination Resistor**

Size: A3 Document Number: **Garda-5** Rev: **SA**

Date: Wednesday, April 26, 2006 Sheet 12 of 46



LED	V	V	V	V
Bluetooth	V	V		
Wireless		V		
Charger			V	
Power2				V



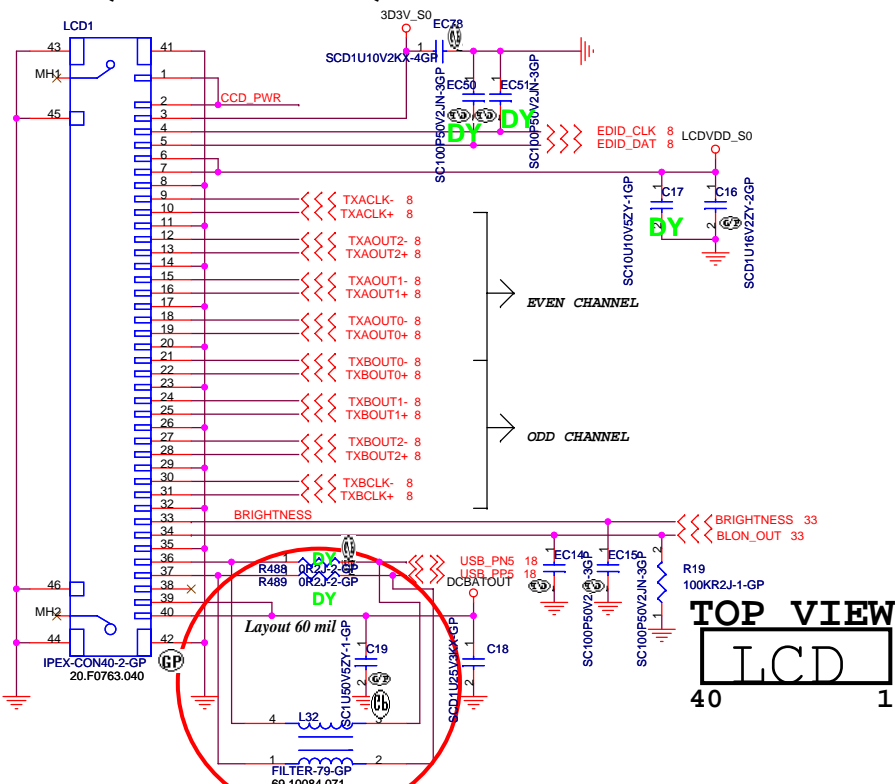
2nd source: 62.40066.001

Pin	Symbol
1	3.3V
2	USB-
3	USB+
4	GND
5	GND

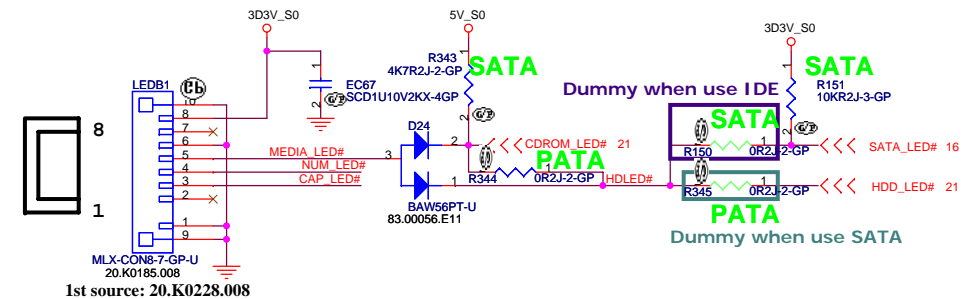
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Pin	Symbol
1	3V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	NC
8	MAIL_LED#
9	PWR_B_LED#
10	NC
11	INT_MICP
12	INT_MICIN

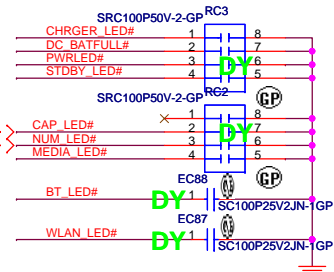
LCD / INVERTER / CCD CONN



LED BD CONN



1st source: 20.K0228.008



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD / LAUNCH / LEDs**

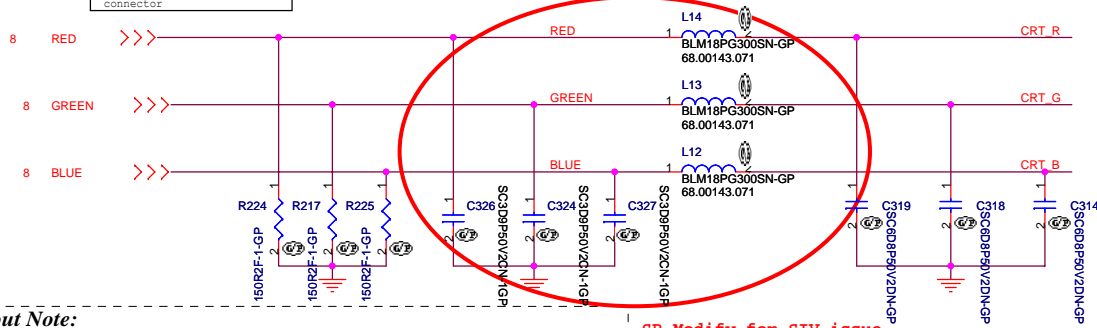
Size: A3 Document Number: **Gards-5** Rev: **-1**

Date: Wednesday, April 26, 2006 Sheet 13 of 46

CRT I/F & CONNECTOR

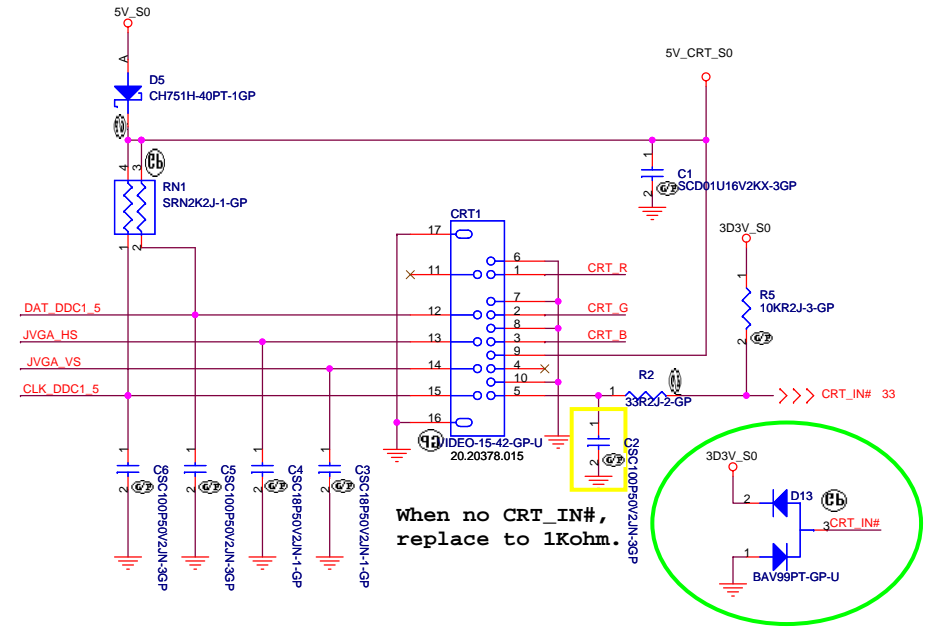
Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 30 ohm@100MHz.



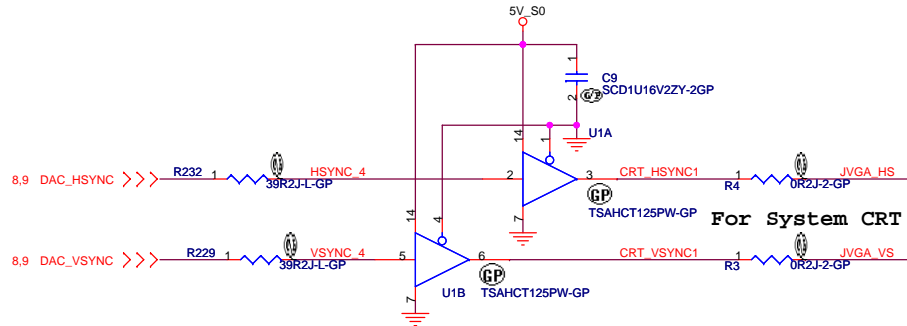
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

SB Modify for SIV issue

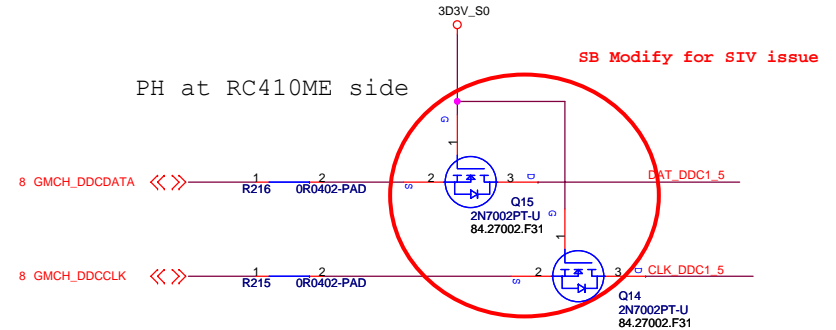


When no CRT_IN#,
replace to 1kOhm.

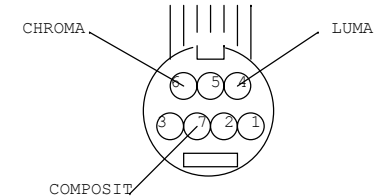
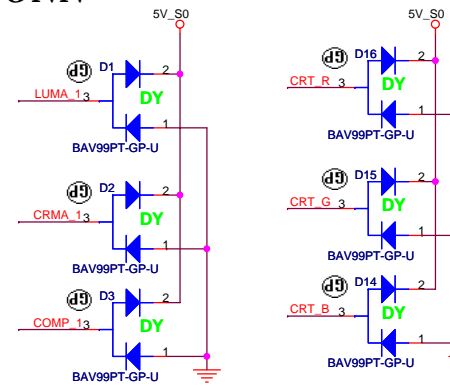
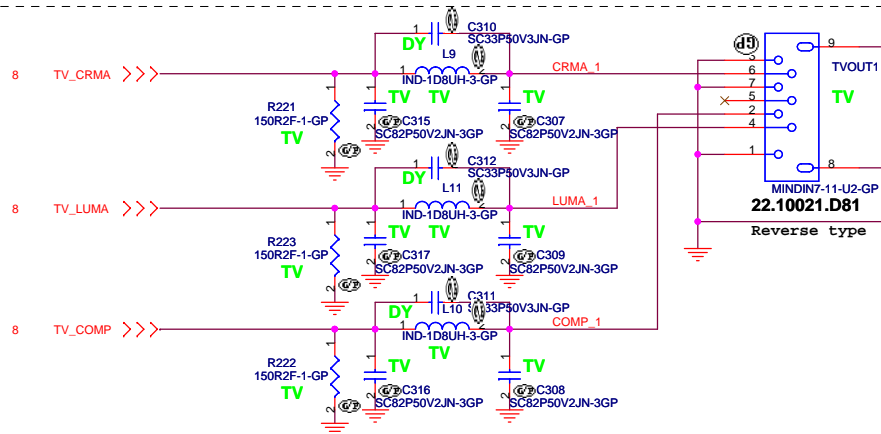
Hsync & Vsync level shift



DDC_CLK & DATA level shift



TV OUT CONN

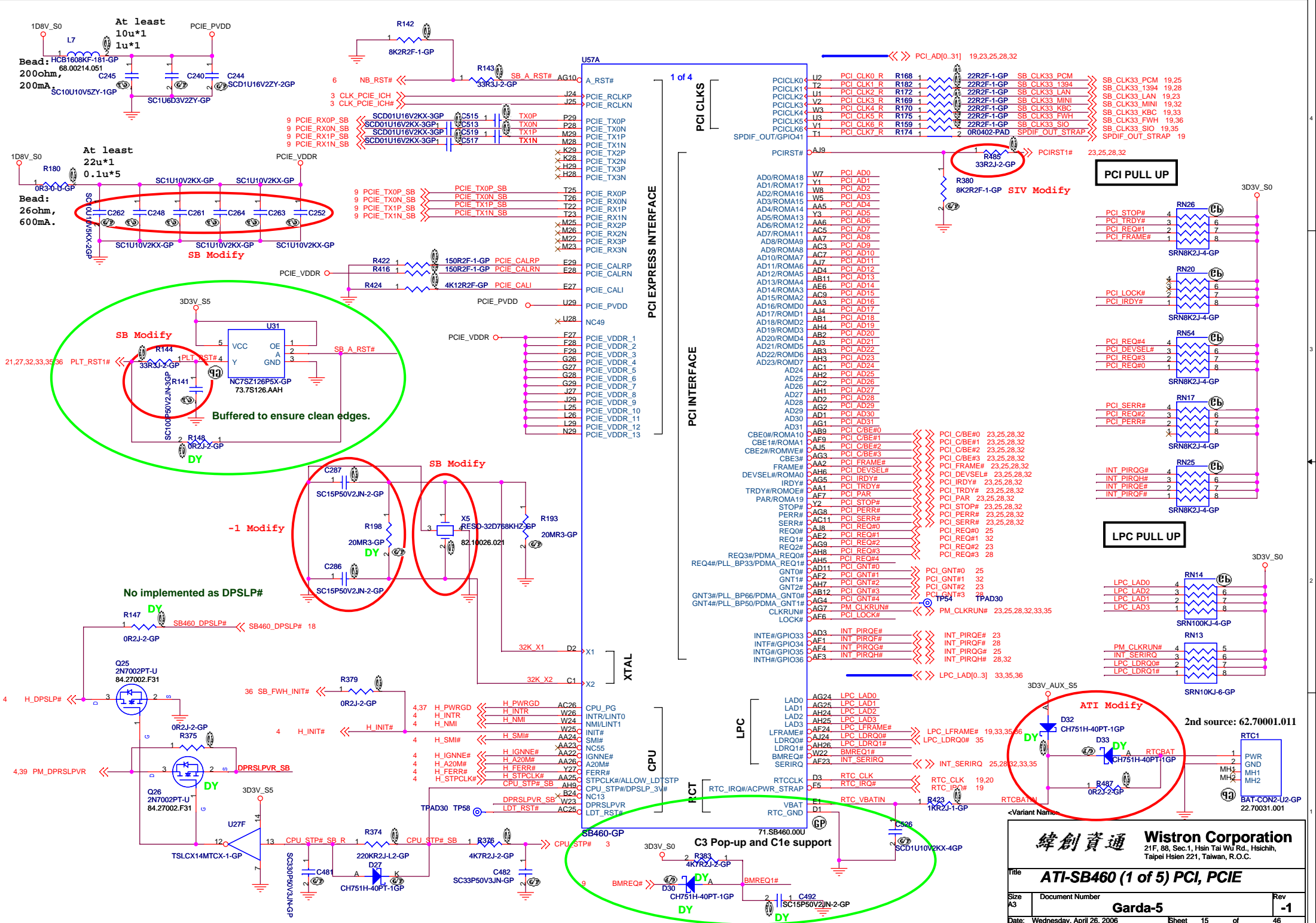


<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT/TV Connector**

Size: A3	Document Number: Garda-5	Rev: SB
Date: Wednesday, April 26, 2006	Sheet 14 of 46	

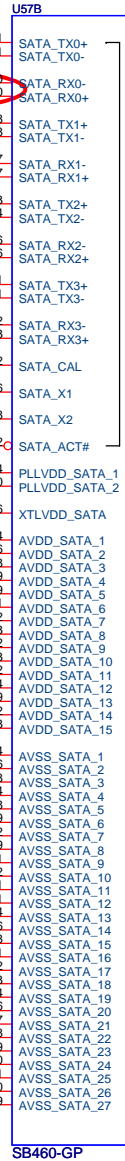
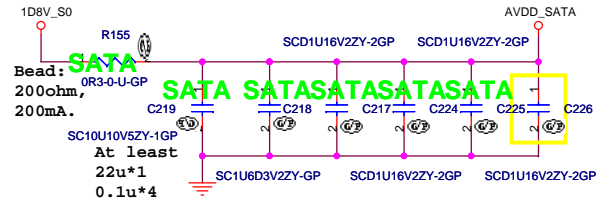
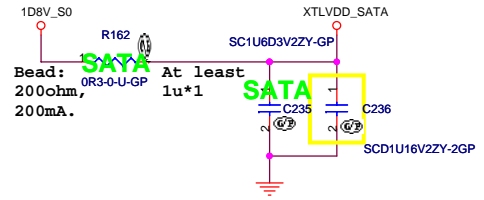
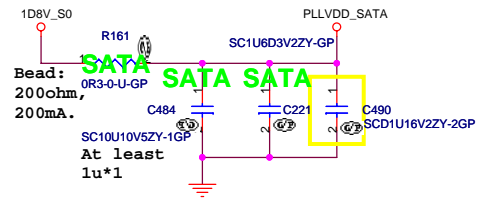
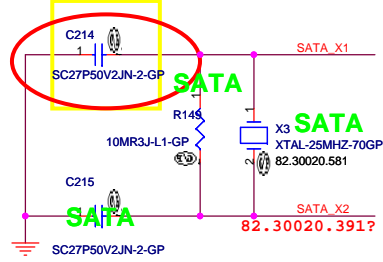




When no SATA replace to 0 ohm.



SB Modify



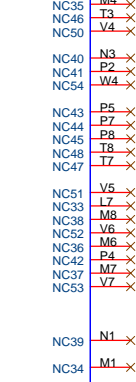
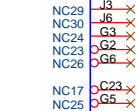
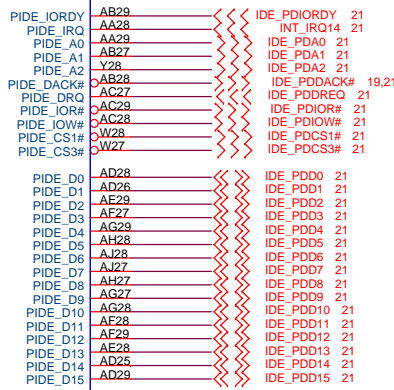
SERIAL ATA

ATA 66/100

SERIAL ATA POWER

SPI ROM

HW MONITOR (SB600)



<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

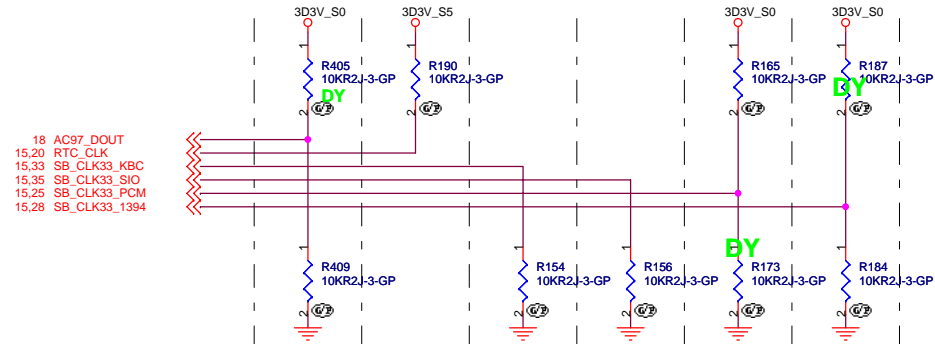
ATI-SB460 (2 of 5) IDE/SATA

Garda-5

SB

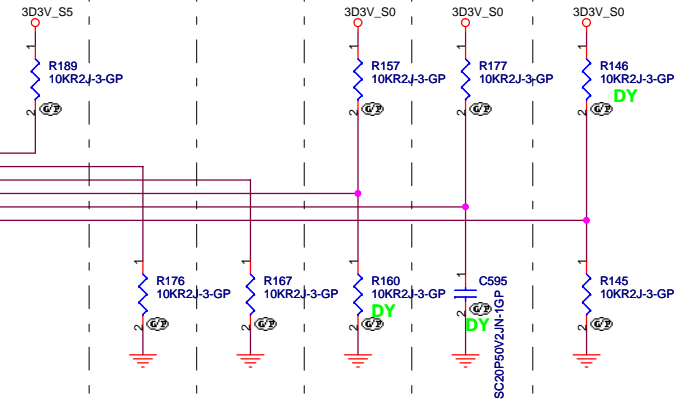
Date: Wednesday, April 26, 2006 Sheet 16 of 46

REQUIRED STRAPS



18 AC97_DOUT
15,20 RTC_CLK
15,33 SB_CLK33_KBC
15,35 SB_CLK33_SIO
15,25 SB_CLK33_PCM
15,28 SB_CLK33_1394

15 RTC_IRQ#
15 SPDIF_OUT_STRAP
15,23 SB_CLK33_LAN
15,32 SB_CLK33_MINI
15,36 SB_CLK33_FWH
15,33,35,36 LPC_LFRAME#



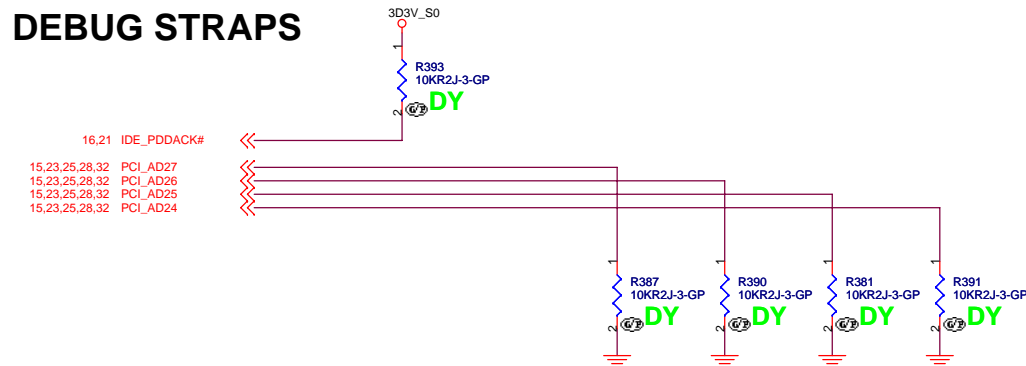
	SB460				SB600	
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. USB PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM H, L = LPC ROM L, L = FWH ROM DEFAULT
PULL LOW	DISABLE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. USB 48MHZ SOURCE DEFAULT	CPU IF=P4 DEFAULT	L, H = LPC II ROM L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	

Require upper 12 addr bits set to "1".

	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	48M XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE LANE AUTO DETECT DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE LANE FORCING TO 2 LANES DEBUG ONLY	DISABLE THERMTRIP#

USB wake from S5 supported.

DEBUG STRAPS



16,21 IDE_PDDACK#
15,23,25,28,32 PCI_AD27
15,23,25,28,32 PCI_AD26
15,23,25,28,32 PCI_AD25
15,23,25,28,32 PCI_AD24

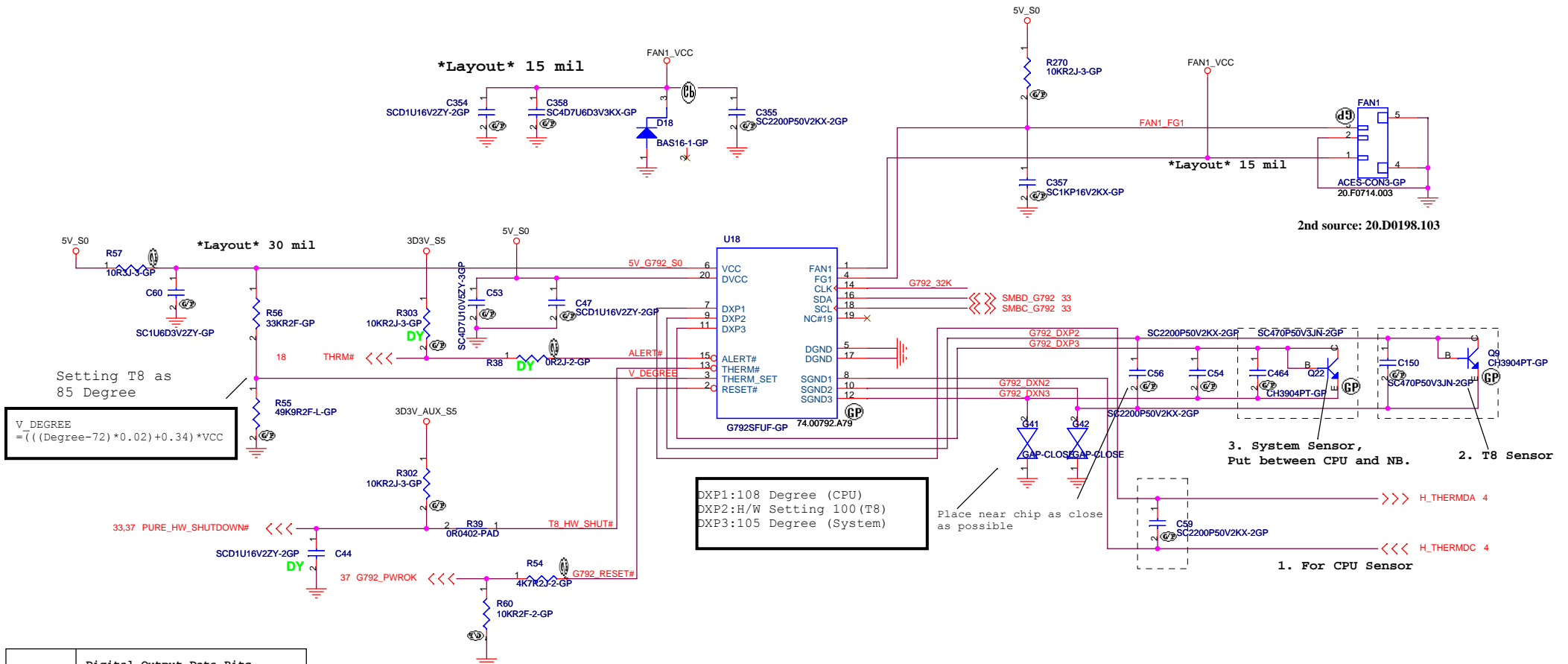
	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT		BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	NOTE: FOR SB460, PCI_AD23 IS RESERVED

SB460 ONLY SB600 ONLY

SB600 ONLY

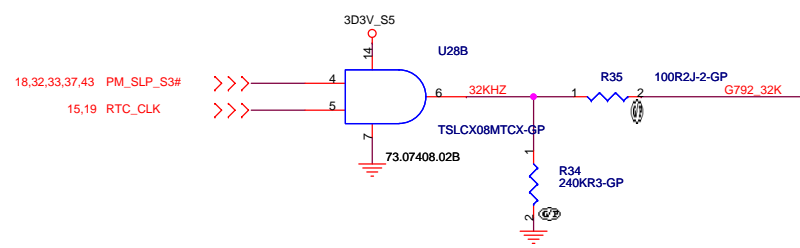
<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.		
ATI-SB460 (5 of 5) STRAPPING				
Title	Document Number			Rev
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Date: Wednesday, April 26, 2006	Sheet 19	of	46	



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

32K suspend clock output



<Variant Name>

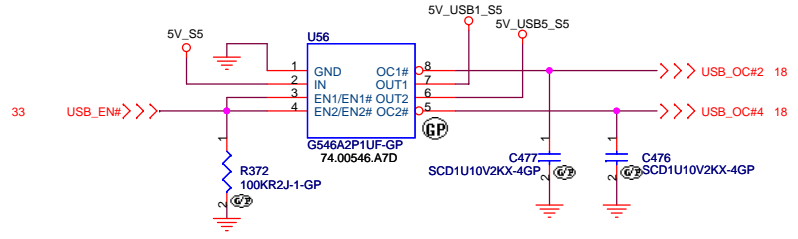
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal/Fan Controller G792**

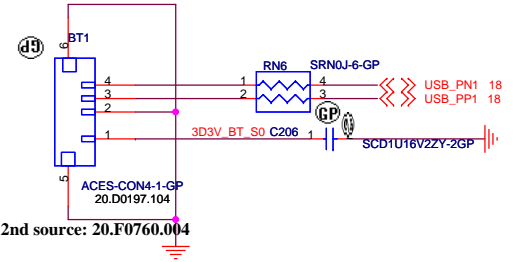
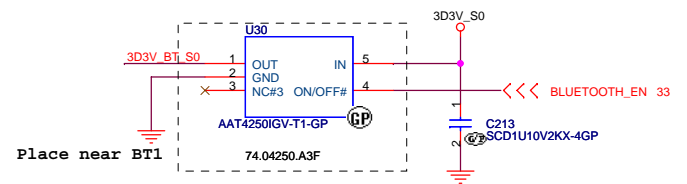
Size Custom: **Garda-5** Document Number: **SA** Rev: **SA**

Date: Wednesday, April 26, 2006 Sheet 20 of 46

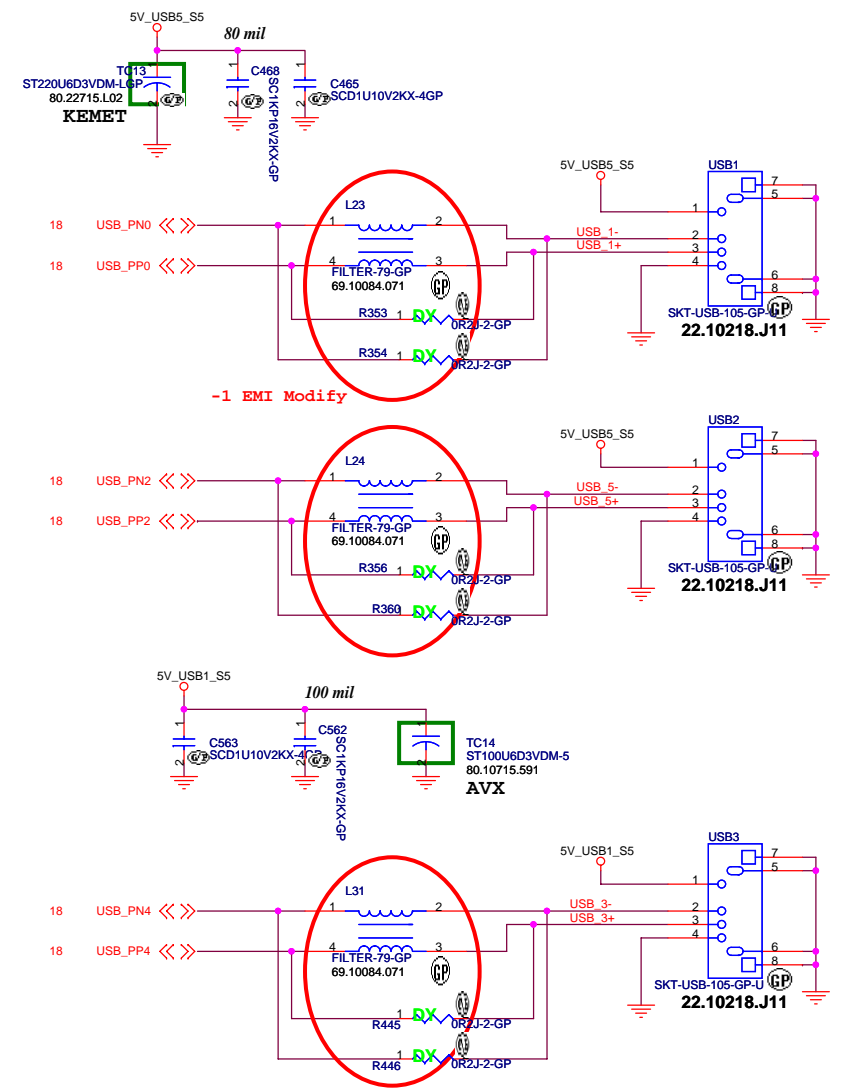
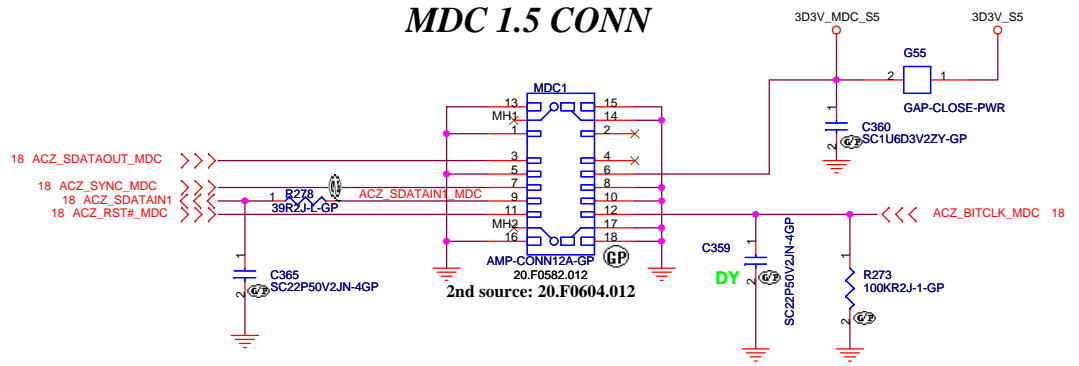
USB PORT



BLUETOOTH MODULE CONNECTOR

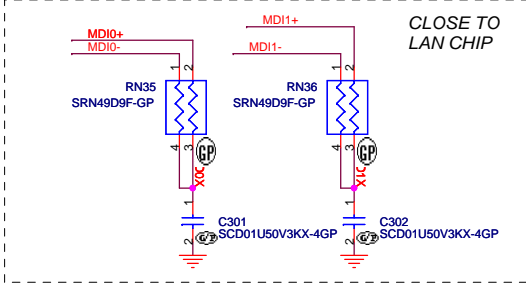


MDC 1.5 CONN

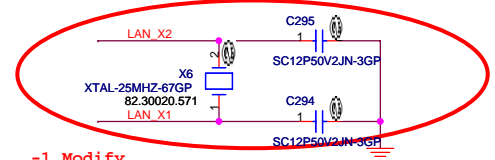


<Variant Name>

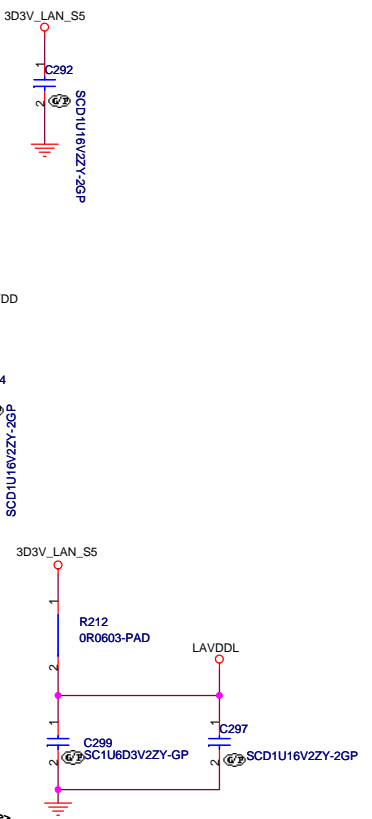
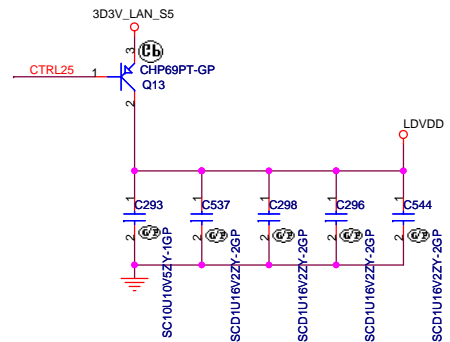
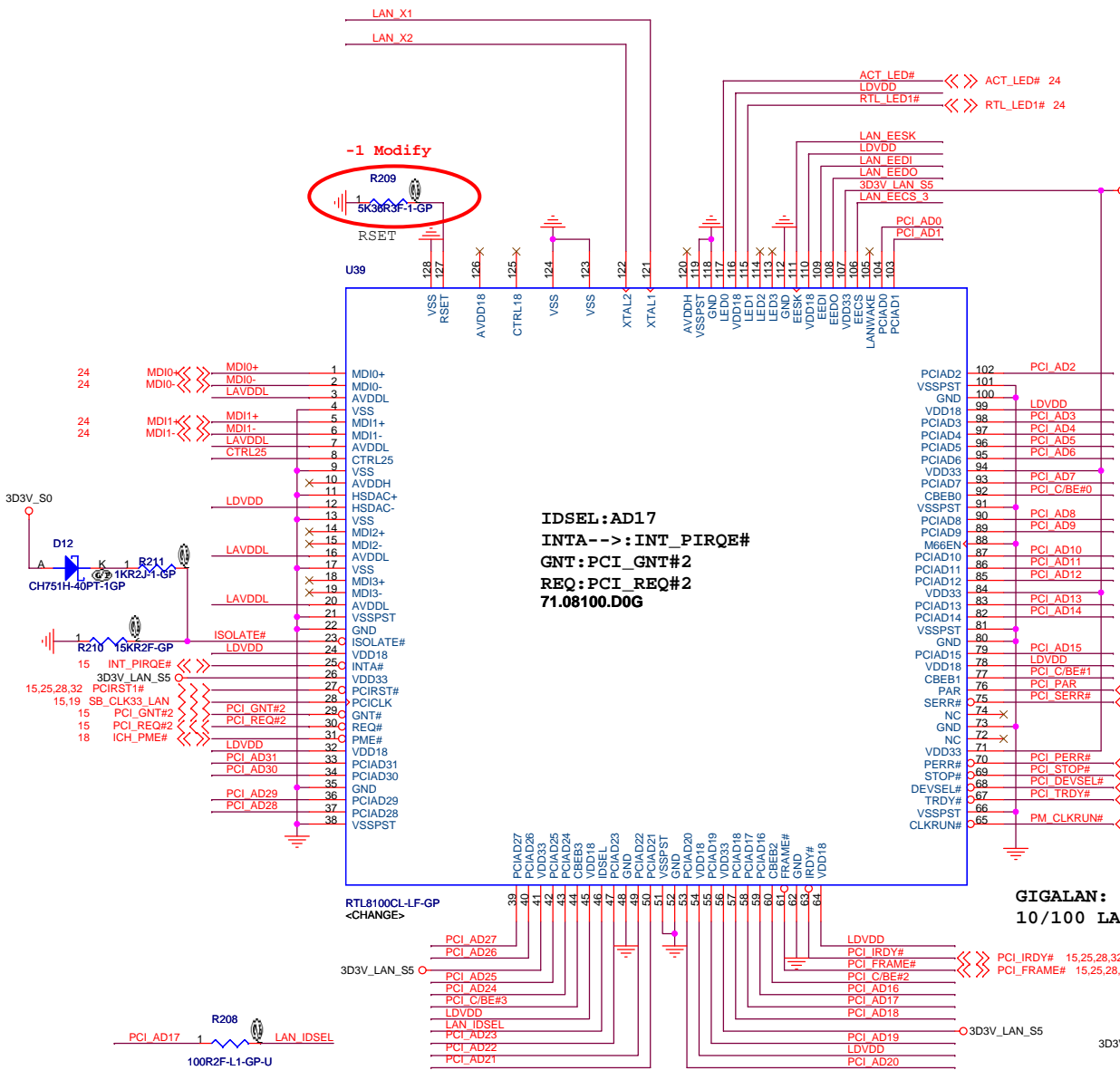
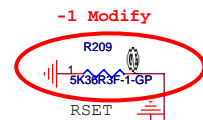
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB and MDC I/F	
Size A3	Document Number
Date: Wednesday, April 26, 2006	Garda-5
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of 46	



15,25,28,32 PCI_C/BE#[3..0] <<< <<<
 15,19,25,28,32 PCI_AD#[31..0] <<< <<<



EEPROM LED OPTION USE '01'
 (DEFINED IN SPEC)
 => LED0 : ACT
 => LED1 : LINK
 (BOTH 10/100 AND GIGA CHIP)



<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

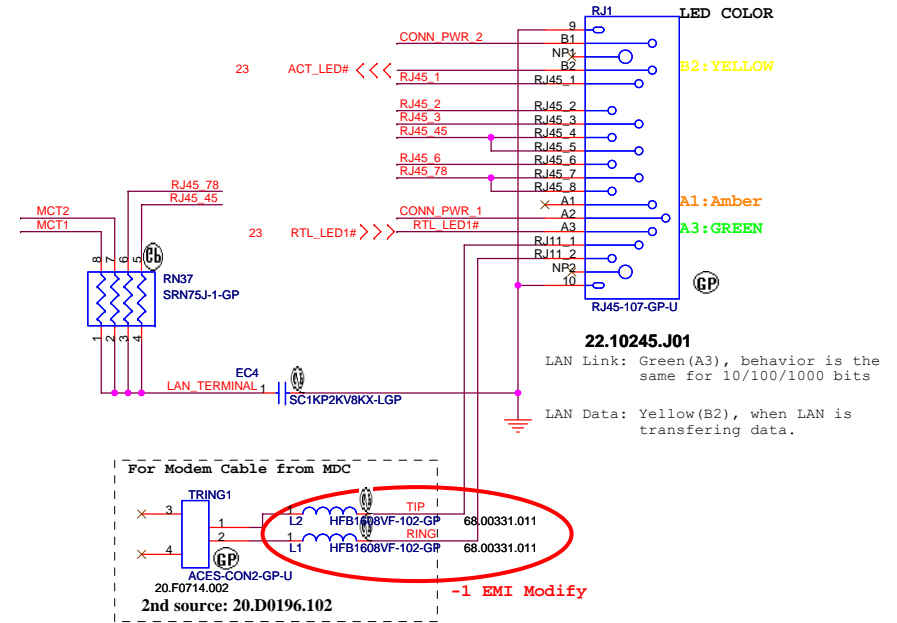
Title: 8100CL

Size A3 Document Number: Garda-5

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Rev -1

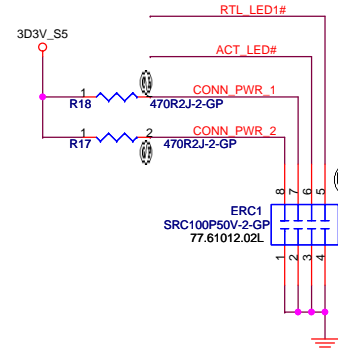
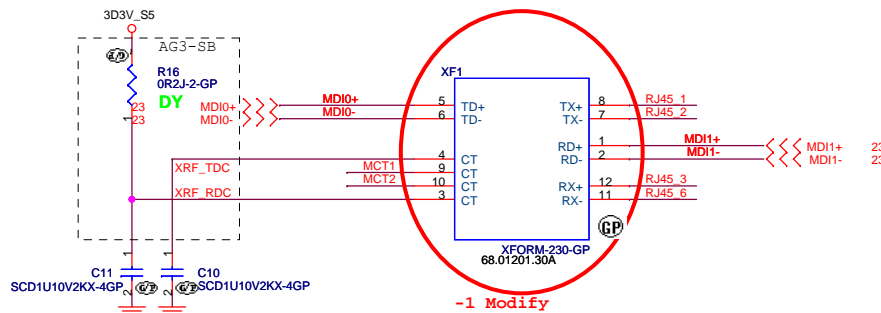
LAN Connector



1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP, DOC_RING, TIP, RING:
 W/S : 10/100 @ Surface layers
 10/20 @ Inner layers



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

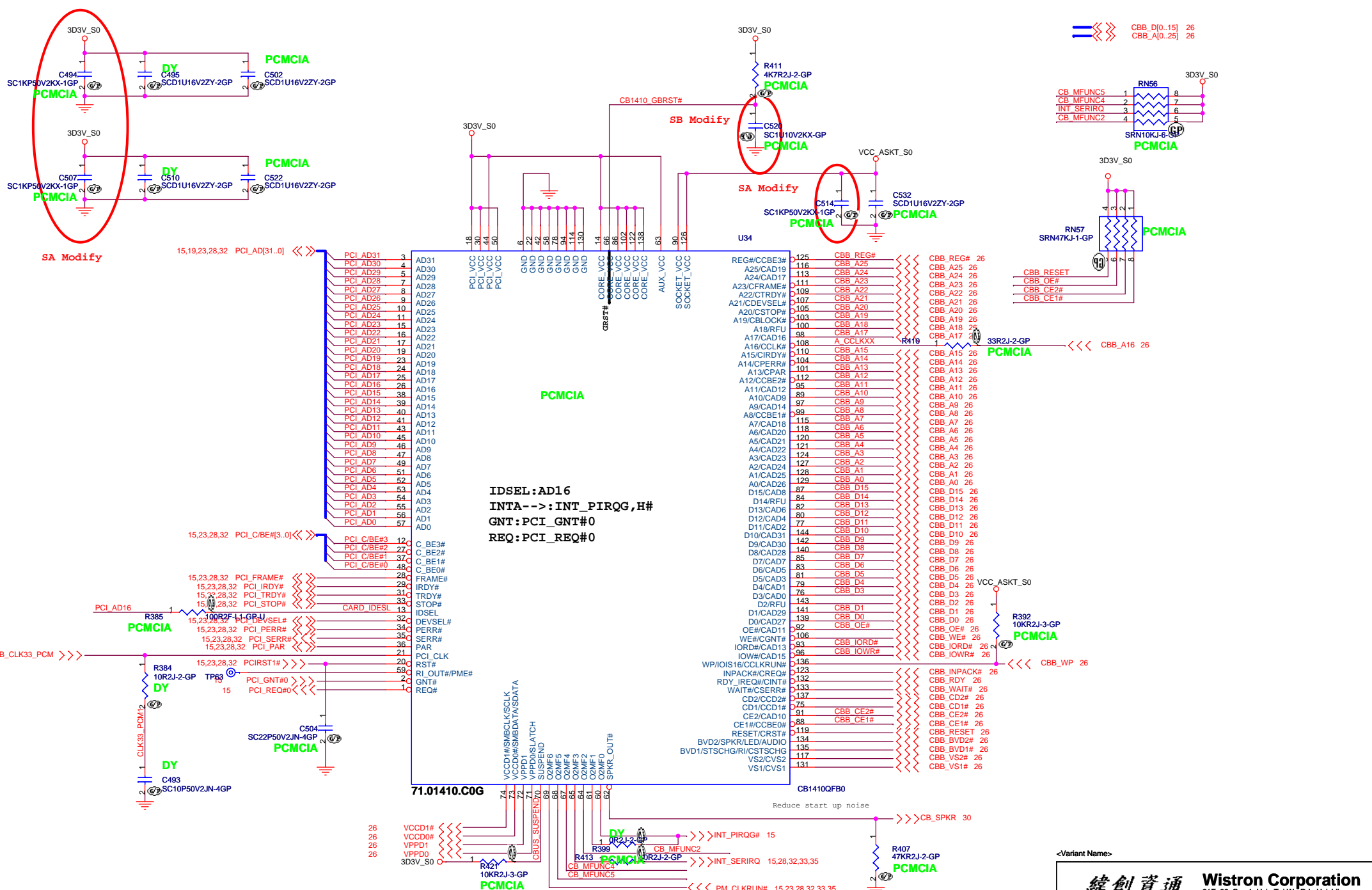
<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

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PCMCIA

IDSEL:AD16
INTA-->:INT_PIRQ,H#
GNT:PCI_GNT#0
REQ:PCI_REQ#0

REG#/CBBE3#	D125	CBB REG#	CBB REG# 26
A25/CAD19	116	CBB A25	CBB A25 26
A24/CAD17	113	CBB A24	CBB A24 26
A23/CFRAME#	111	CBB A23	CBB A23 26
A22/CTRDY#	107	CBB A21	CBB A22 26
A21/CDEVSEL#	105	CBB A20	CBB A21 26
A20/GSTOP#	103	CBB A19	CBB A19 26
A19/CLOCK#	100	CBB A18	CBB A18 26
A17/CAD16	98	CBB A17	CBB A17 26
A16/CCLK#	108	CBB A15	CBB A15 26
A15/CIRDY#	104	CBB A14	CBB A14 26
A14/CPERR#	101	CBB A13	CBB A13 26
A13/CPAR#	102	CBB A12	CBB A12 26
A12/CCEB2#	112	CBB A11	CBB A11 26
A11/CAD12	95	CBB A10	CBB A10 26
A10/CAD9	89	CBB A9	CBB A9 26
A9/CAD14	97	CBB A8	CBB A8 26
A8/CCEB1#	115	CBB A7	CBB A7 26
A7/CAD18	118	CBB A6	CBB A6 26
A6/CAD21	120	CBB A5	CBB A5 26
A4/CAD22	121	CBB A4	CBB A4 26
A3/CAD23	124	CBB A3	CBB A3 26
A2/CAD24	128	CBB A2	CBB A2 26
A1/CAD25	129	CBB A1	CBB A1 26
A0/CAD26	127	CBB A0	CBB A0 26
D15/CAD8	87	CBB D15	CBB D15 26
D14/RFU	84	CBB D14	CBB D14 26
D13/CAD6	82	CBB D13	CBB D13 26
D12/CAD4	80	CBB D12	CBB D12 26
D11/CAD2	77	CBB D11	CBB D11 26
D10/CAD31	144	CBB D10	CBB D10 26
D9/CAD30	142	CBB D9	CBB D9 26
D8/CAD28	140	CBB D8	CBB D8 26
D7/CAD7	85	CBB D7	CBB D7 26
D6/CAD5	83	CBB D6	CBB D6 26
D5/CAD3	81	CBB D5	CBB D5 26
D4/CAD1	79	CBB D4	CBB D4 26
D3/CAD0	76	CBB D3	CBB D3 26
D2/RFU	143	CBB D2	CBB D2 26
D1/CAD29	141	CBB D1	CBB D1 26
D0/CAD27	139	CBB D0	CBB D0 26
OE#/CAD11	92	CBB OE#	CBB OE# 26
WE#/CGNT#	93	CBB IORD#	CBB WE# 26
IORD#/CAD13	96	CBB LOWR#	CBB IORD# 26
IOW#/CAD15	96	CBB LOWR#	CBB IOWR# 26
WP/IOIS16/CCLKRUN#	136	CBB INPACK#	CBB WP 26
INPACK#/CREQ#	123	CBB RDY	CBB INPACK# 26
RDY_IREQ#/CNT#	133	CBB CD2#	CBB RDY 26
WAIT#/CSERR#	137	CBB CD1#	CBB WAIT# 26
CD2/CCD2#	75	CBB CE2#	CBS CD2# 26
CD1/CCD1#	91	CBB CE1#	CBB CD1# 26
CE2/CAD10	88	CBB CE1#	CBB CE2# 26
CE1/CCEB0#	88	CBB CE1#	CBB CE1# 26
RESET/CRST#	119	CBB RESET	CBB RESET 26
BVD2/SPKR/LED/AUDIO	134	CBB BVD2#	CBB BVD2# 26
BVD1/STSCHG/RI/CTS/CHG	135	CBB BVD1#	CBB BVD1# 26
VS2/CV52	117	CBB VS2#	CBB VS2# 26
VS1/CV51	131	CBB VS1#	CBB VS1# 26

CBB_D[0..15] 26
 CBB_A[0..25] 26

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **CardBus_ENE CB1410**

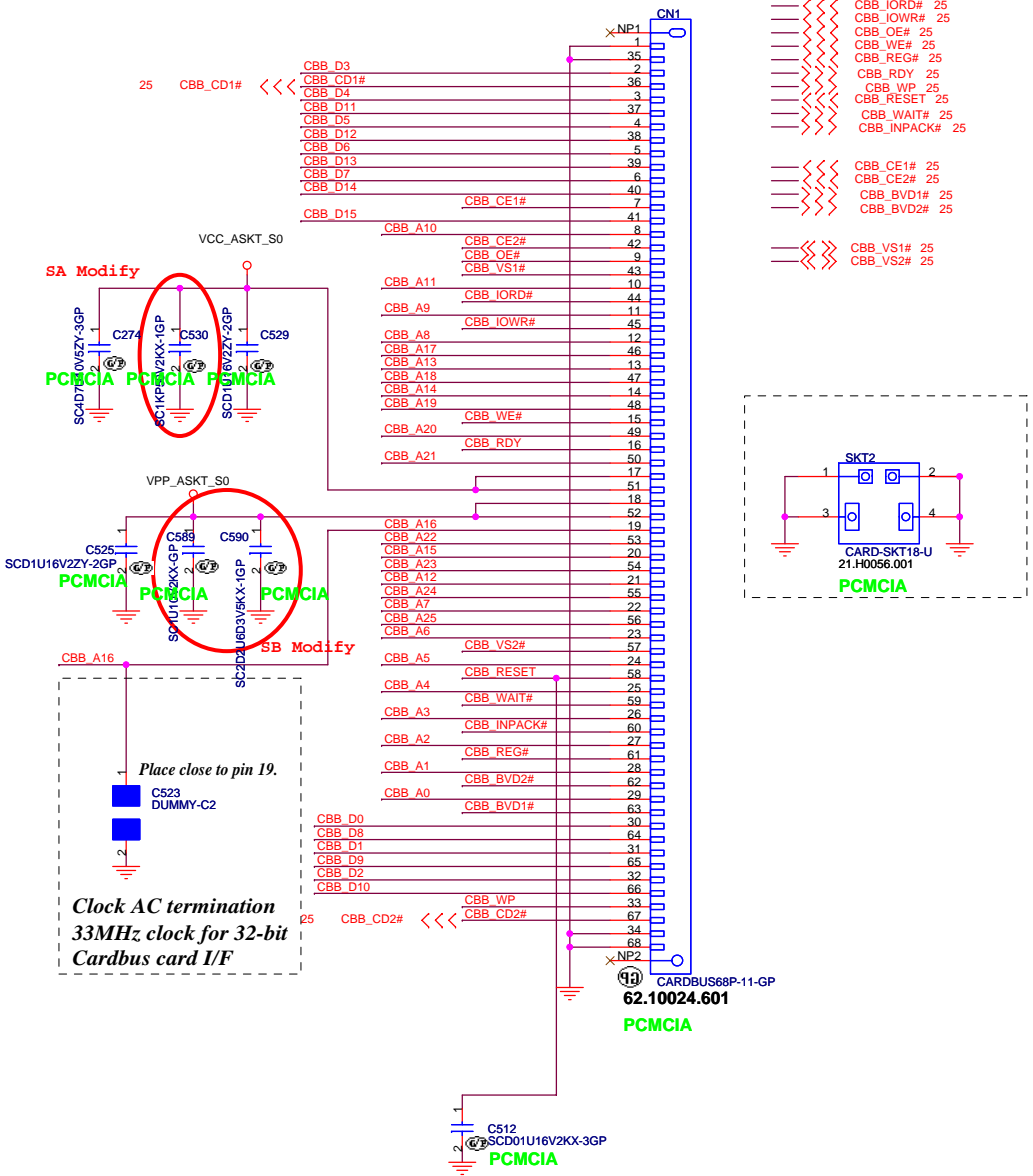
Size A3 Document Number **Garda-5** Rev **SA**

Date: Wednesday, April 26, 2006 Sheet 26 of 46

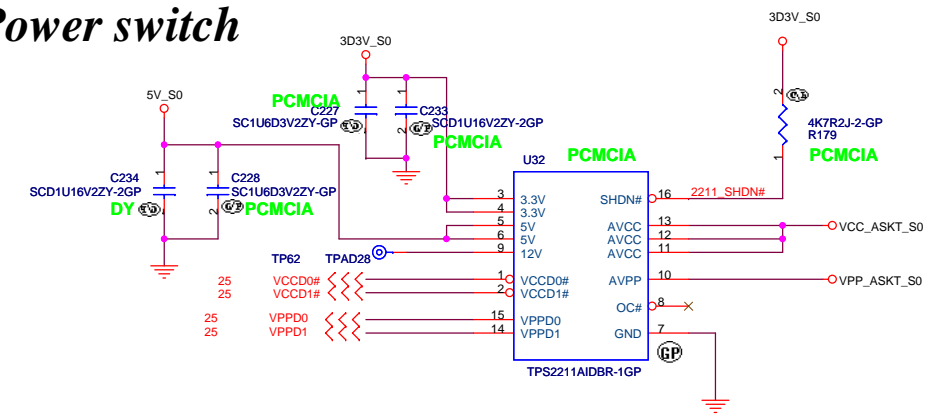
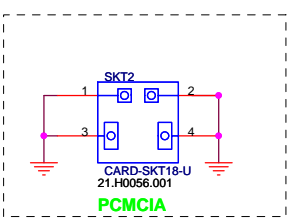
PCMCIA Socket

Cardbus I/F

Power switch



- CBB_D[0..15] 25
 CBB_A[0..25] 25
- CBB_IORD# 25
 CBB_IOWR# 25
 CBB_OE# 25
 CBB_WE# 25
 CBB_REG# 25
 CBB_RDY 25
 CBB_WP 25
 CBB_RESET# 25
 CBB_WAIT# 25
 CBB_INPACK# 25
- CBB_CE1# 25
 CBB_CE2# 25
 CBB_BVD1# 25
 CBB_BVD2# 25
- CBB_VS1# 25
 CBB_VS2# 25



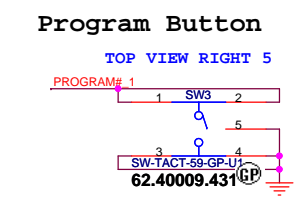
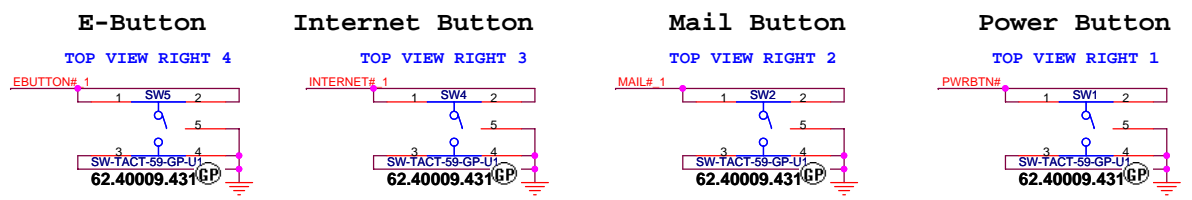
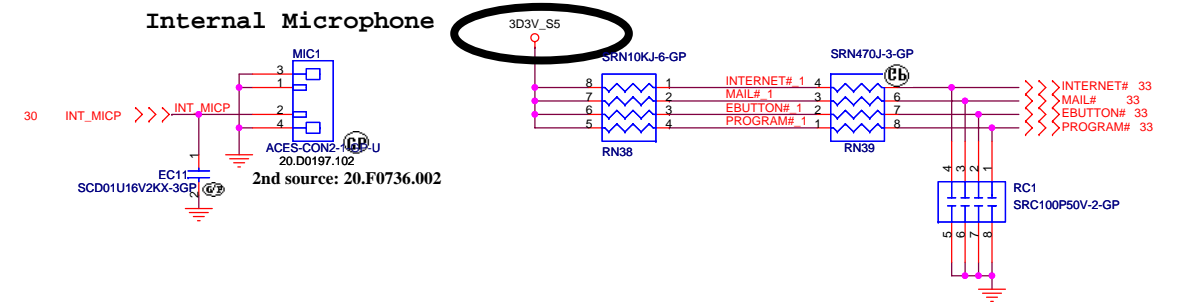
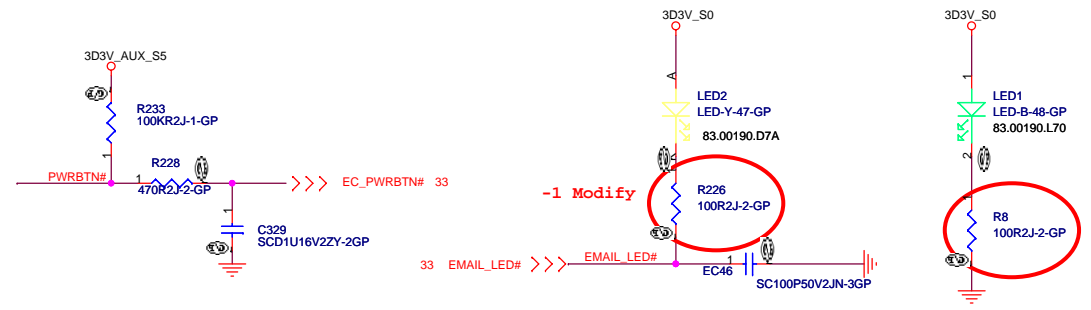
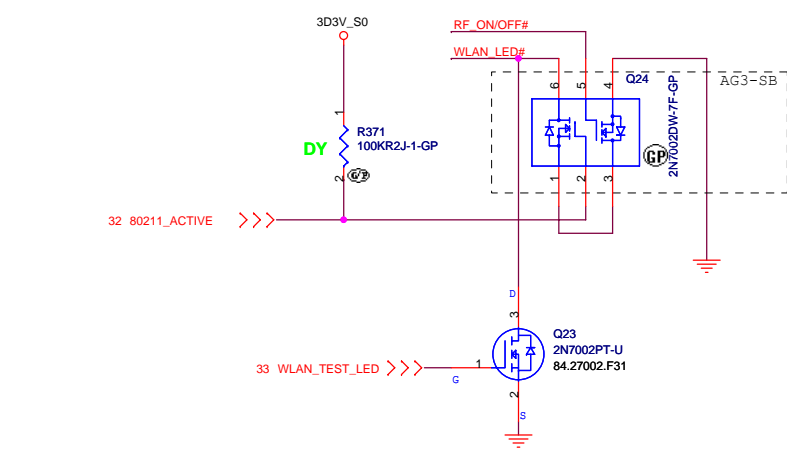
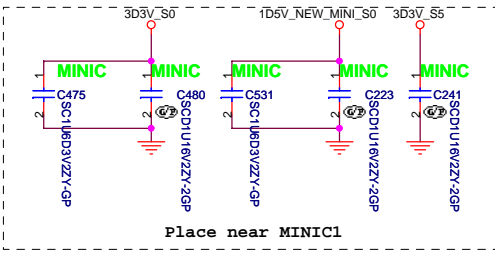
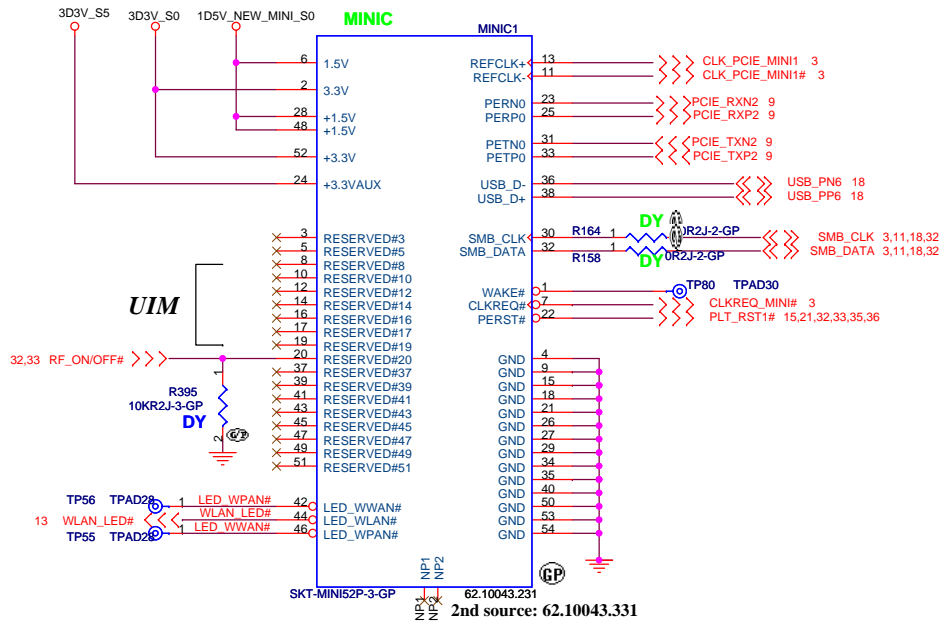
Place close to pin 19.
C523
 DUMMY-C2

Clock AC termination
 33MHz clock for 32-bit
 Cardbus card I/F

<Variant Name>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
PCMCIA	
Title	Document Number
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Mini Card Connector



LED					
Button	V	V	V	V	V
	Program Button	E-Button	Internet Button	Mail Button	Power Button

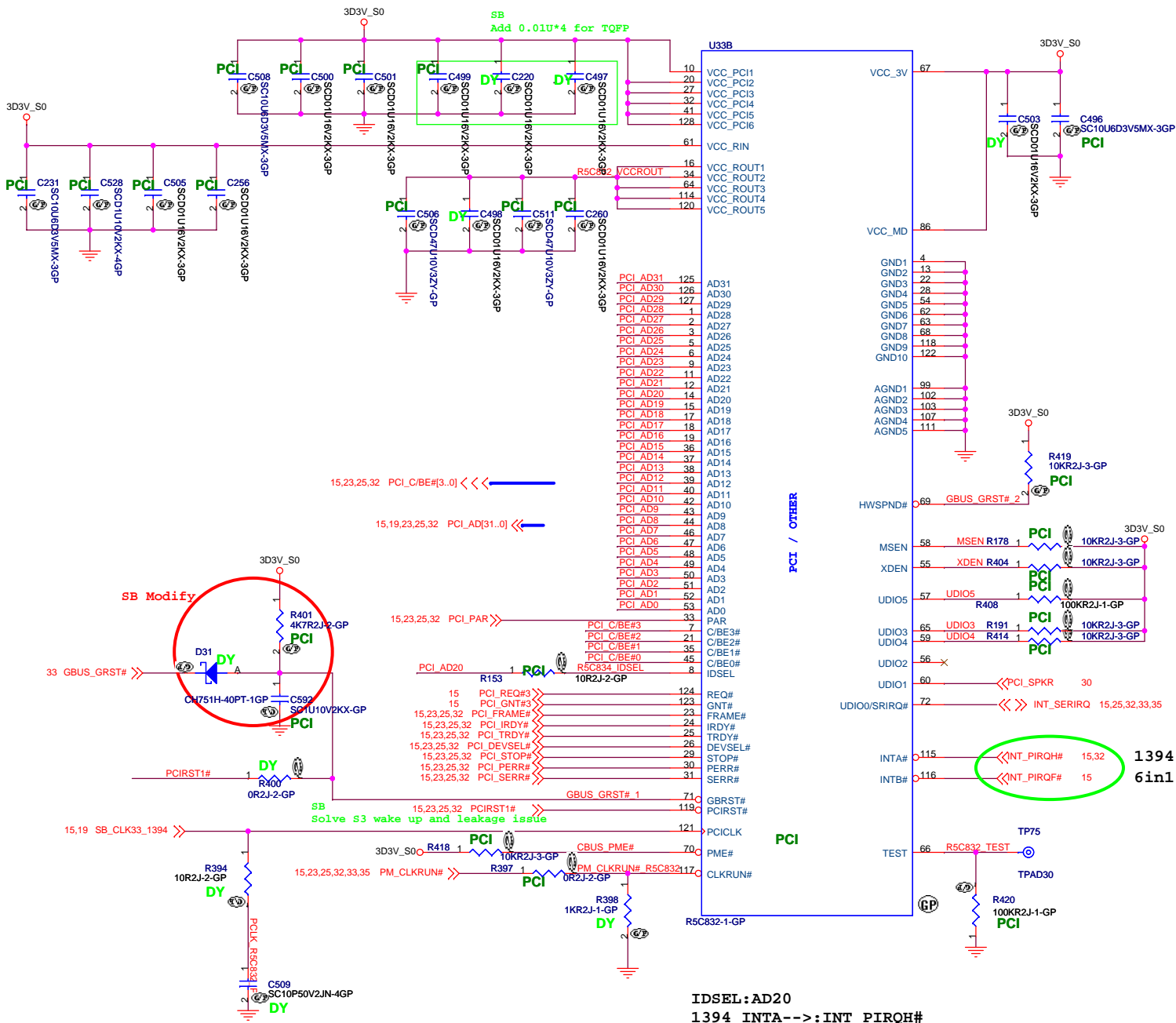
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD / Launch Button**

Size A3 Document Number: **Garda-5** Rev **-1**

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PCI AD31	125	AD31
PCI AD30	128	AD30
PCI AD29	127	AD29
PCI AD28	1	AD28
PCI AD27	2	AD27
PCI AD26	3	AD26
PCI AD25	5	AD25
PCI AD24	6	AD24
PCI AD23	11	AD23
PCI AD22	12	AD22
PCI AD21	14	AD21
PCI AD20	15	AD20
PCI AD19	17	AD19
PCI AD18	18	AD18
PCI AD17	19	AD17
PCI AD16	36	AD16
PCI AD15	37	AD15
PCI AD14	38	AD14
PCI AD13	39	AD13
PCI AD12	40	AD12
PCI AD11	42	AD11
PCI AD10	43	AD10
PCI AD9	44	AD9
PCI AD8	46	AD8
PCI AD7	47	AD7
PCI AD6	48	AD6
PCI AD5	49	AD5
PCI AD4	50	AD4
PCI AD3	51	AD3
PCI AD2	52	AD2
PCI AD1	53	AD1
PCI AD0	7	AD0

PCI / OTHER

IDSEL: AD20
 1394 INTA-->:INT_PIRQH#
 6IN1 INTB-->:INT_PIRQF#
 GNT:PCI_GNT#3
 REQ:PCI_REQ#3

1394 : INTA#
 6in1 : INTB#(INT_PIRQF#)share

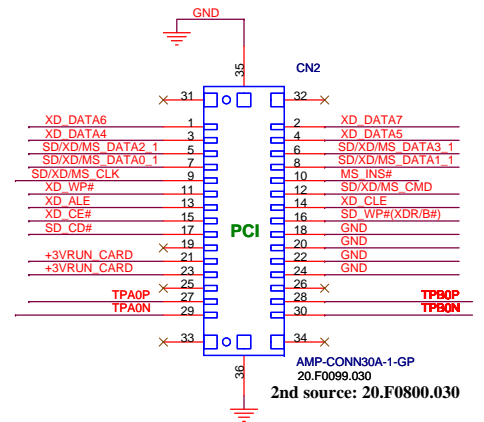
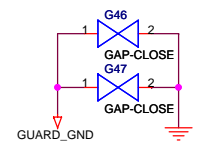
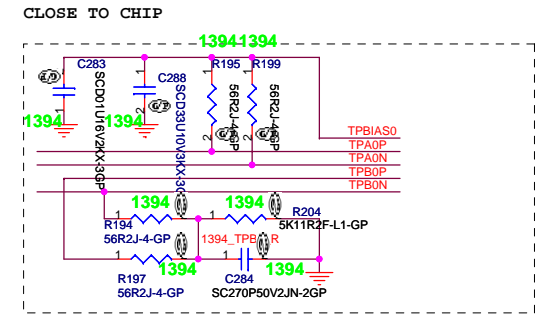
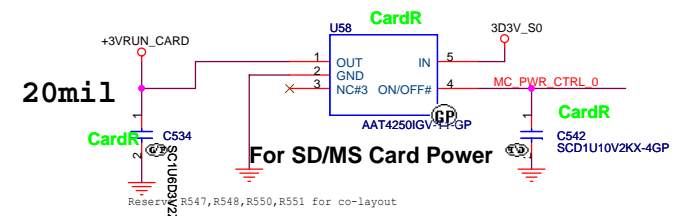
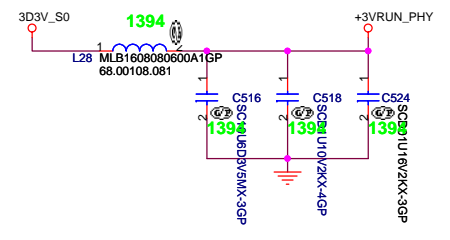
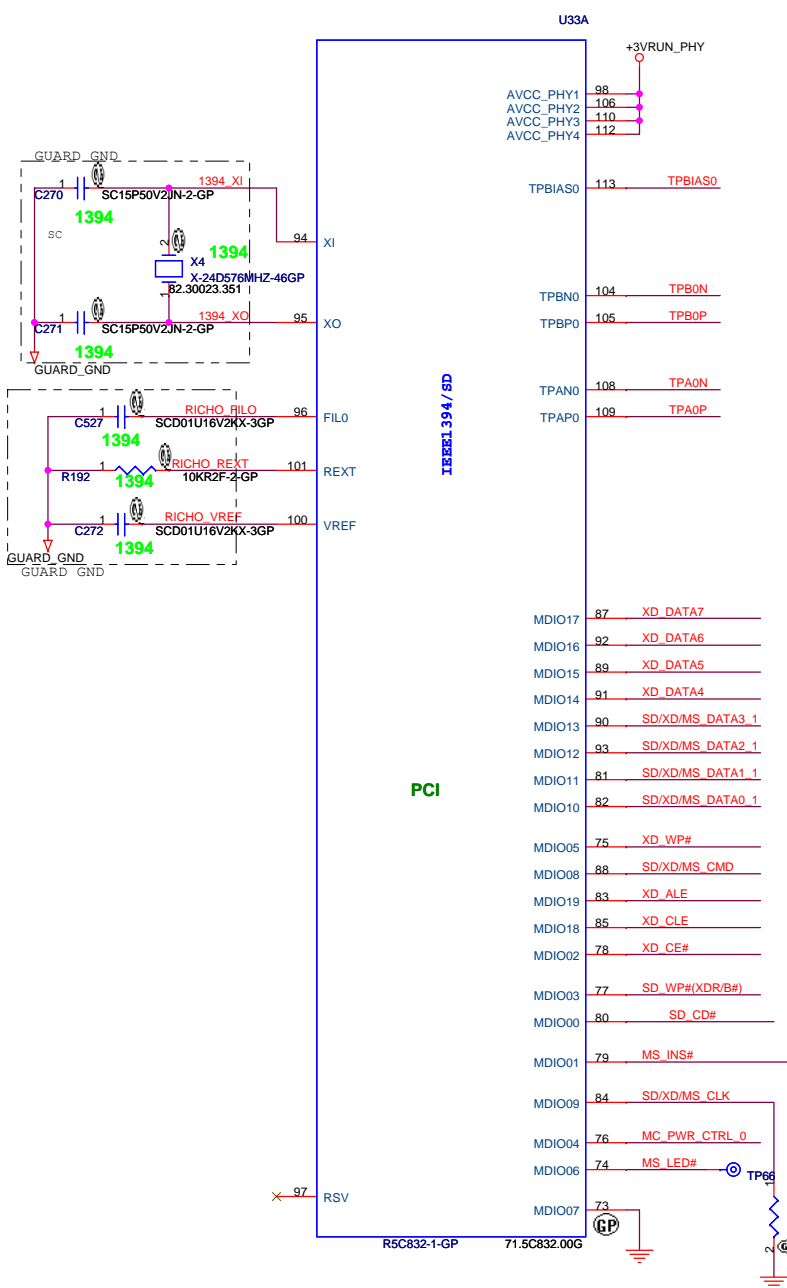
<Variant Name>

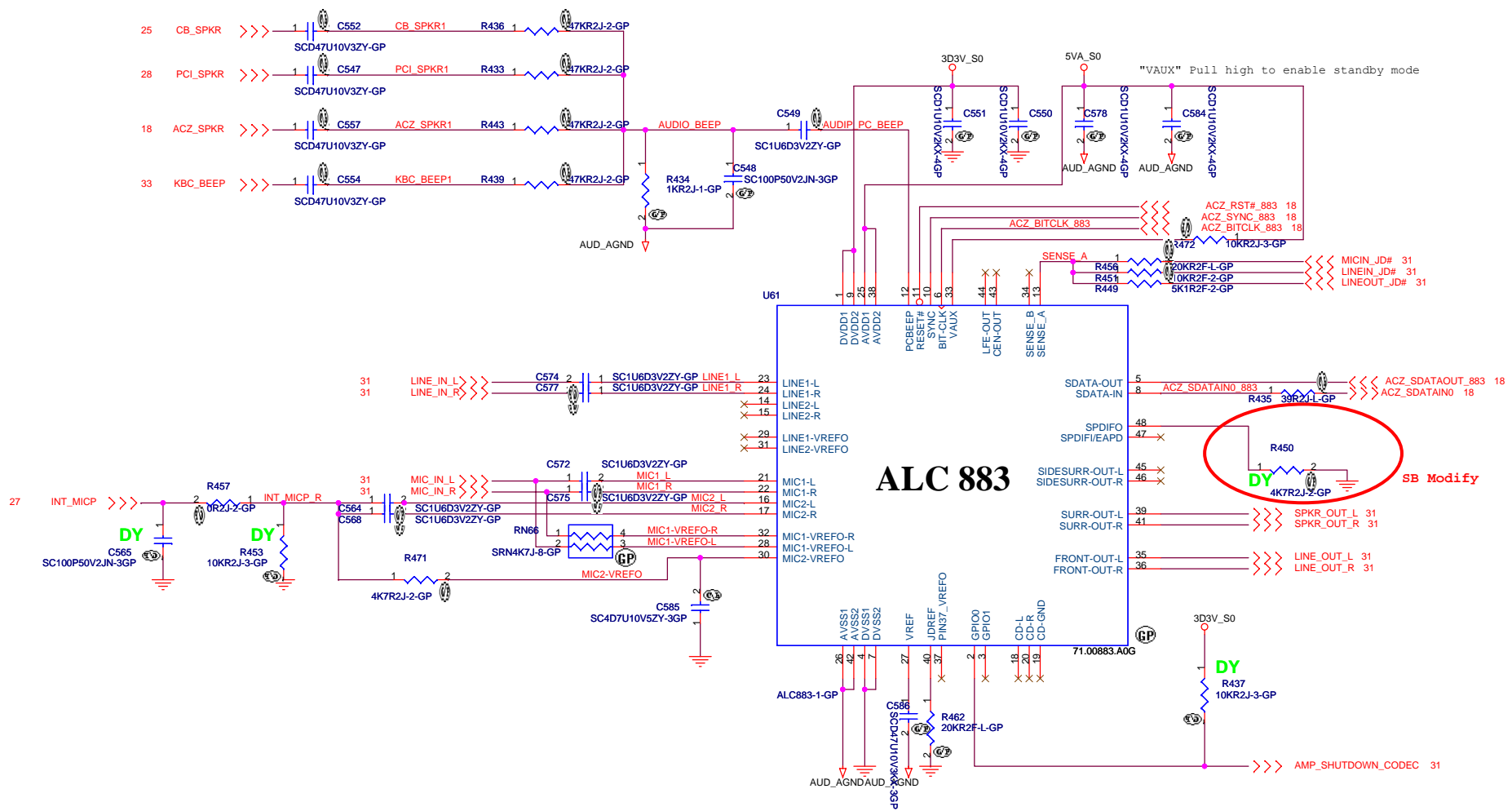
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **R5C832_1394_7IN1(1/2)**

Size A3 Document Number **Garda5** Rev **SB**

Date: Wednesday, April 26, 2006 Sheet 28 of 46

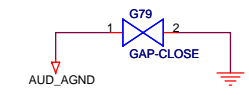
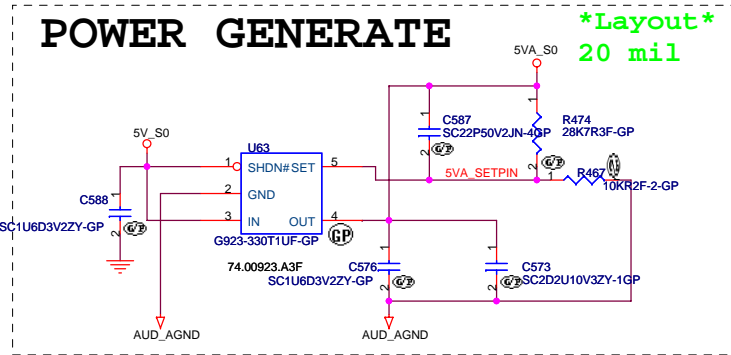




- 1) When GPIO0 is asserted, AMP should be muted.
- 2) SPDIFO should be turned off when not used.

Configuration:
 (3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.)

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP, Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input



<Variant Name>

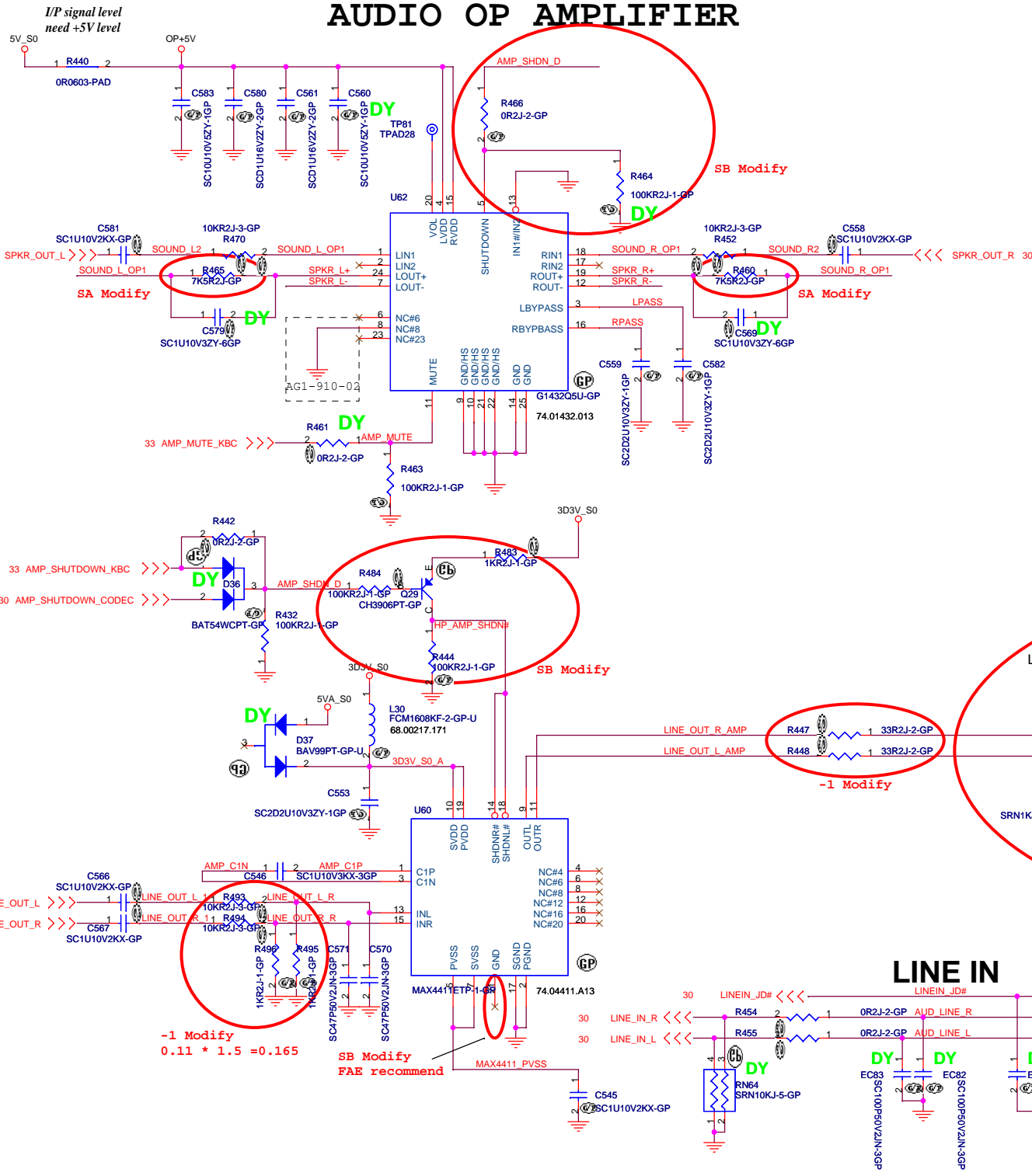
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC883**

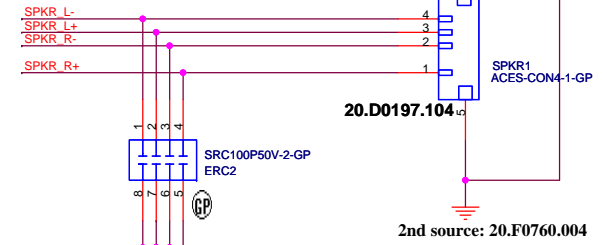
Size A3	Document Number	Rev SB
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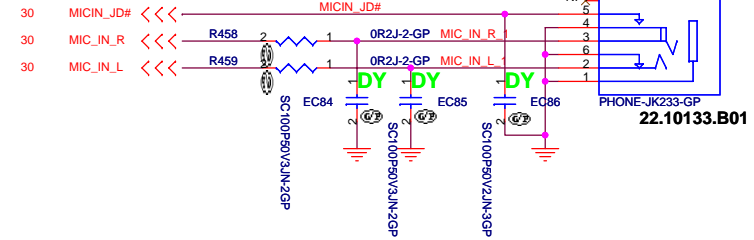
AUDIO OP AMPLIFIER



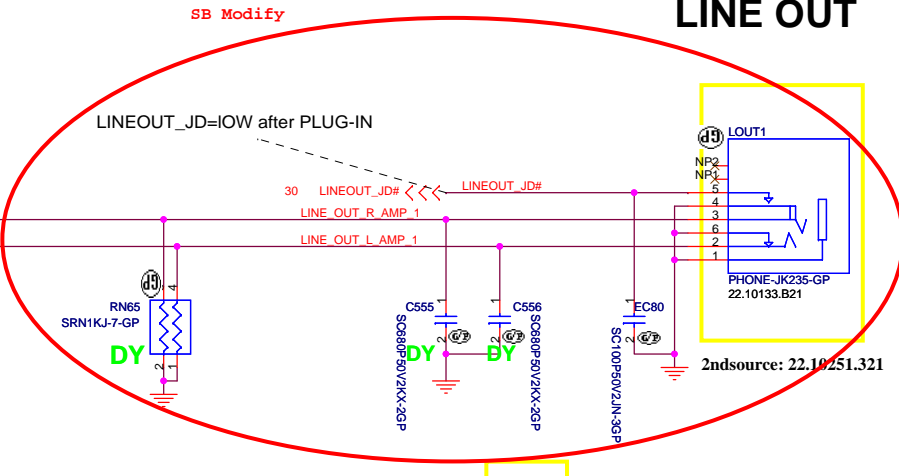
Internal Speaker



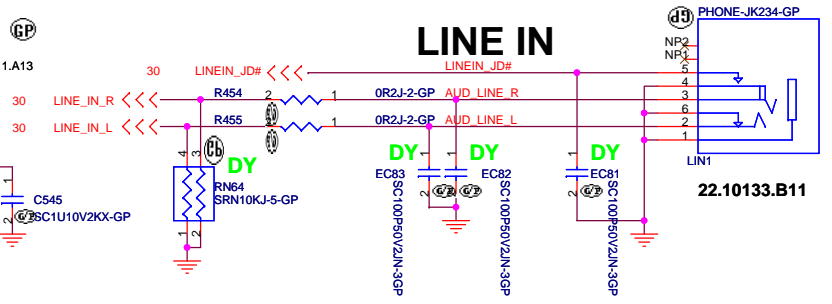
EXT MIC IN



LINE OUT



LINE IN



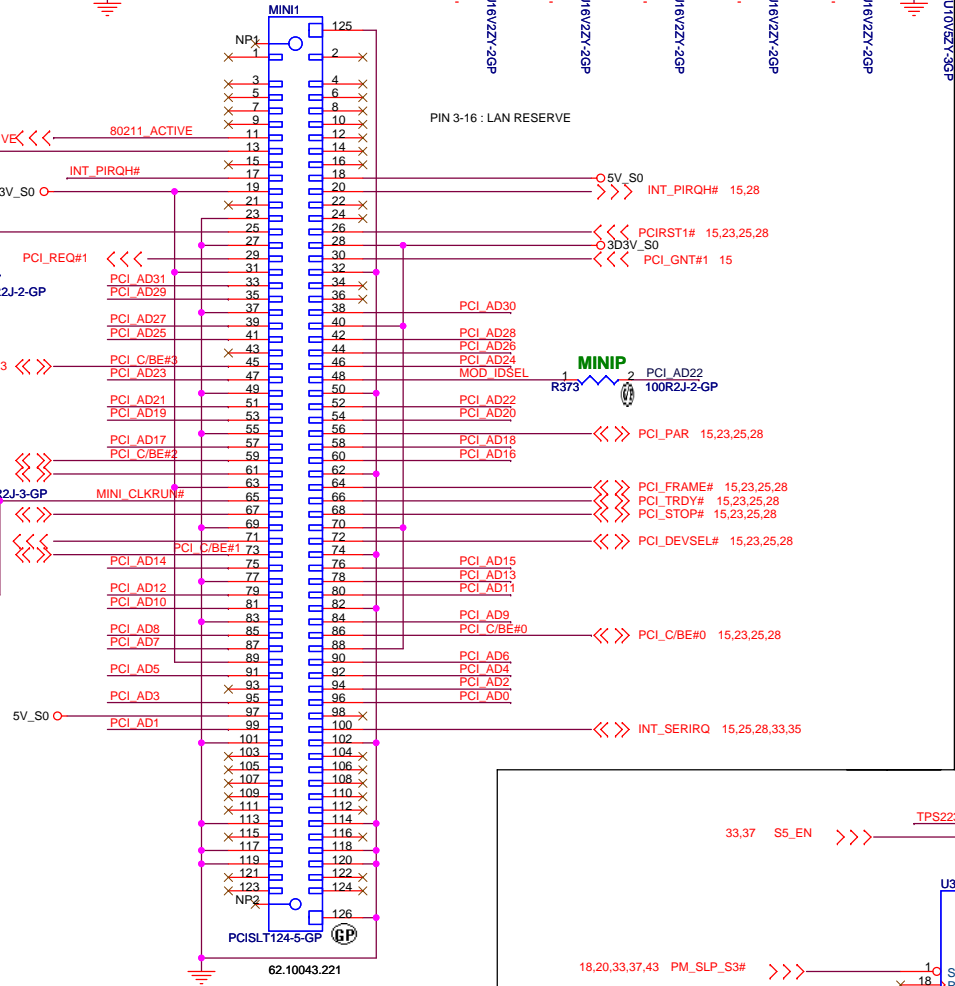
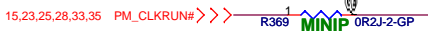
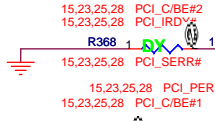
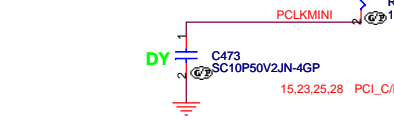
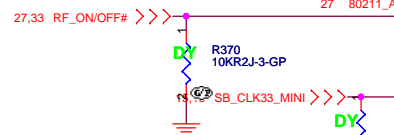
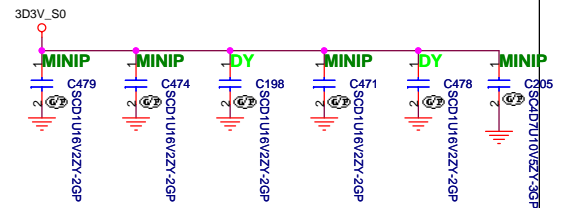
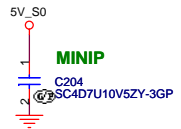
When has SPDIF replace to "22.10205.251".

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Title			
AUDIO AMP AND JACK			
Size	Document Number		Rev
A3		Garda-5	-1
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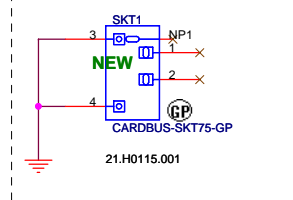
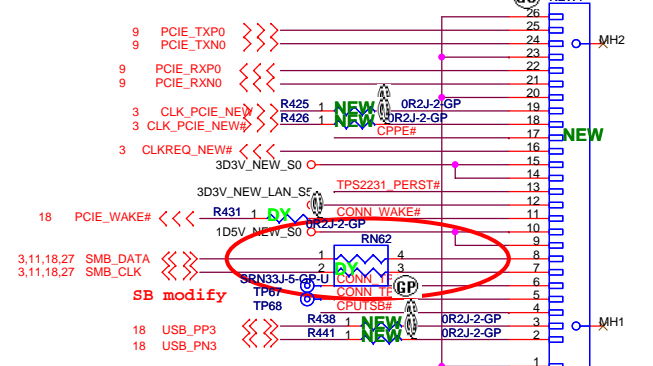
15,19,23,25,28 PCI_AD[0..31]

IDSEL:AD21
INTA-->:INT_PIRQE#
GNT:PCI_GNT1#
REQ:PCI_REQ1#



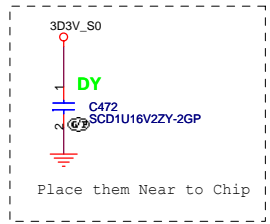
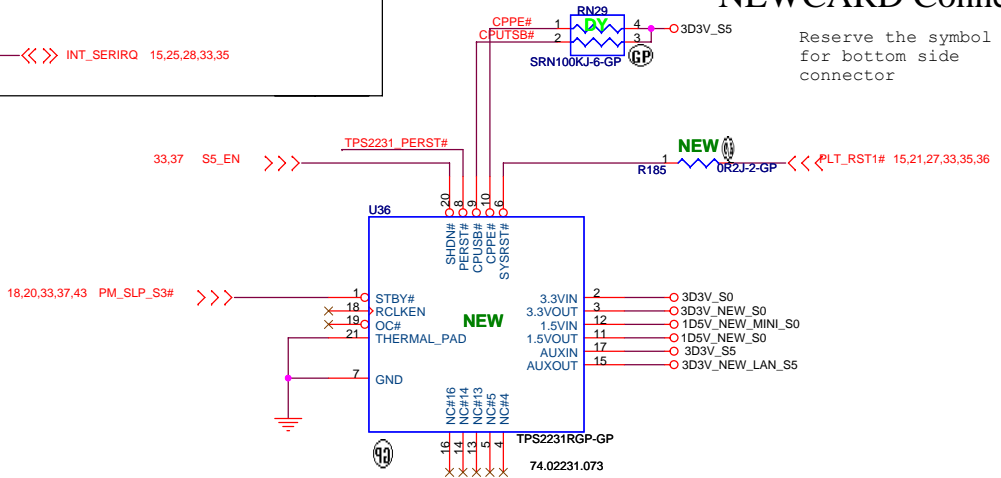
IDSEL:AD22
INTA-->:INT_PIRQG#
INTB-->:INT_PIRQG#
GNT:PCI_GNT#1
REQ:PCI_REQ#1

62.10043.221
2nd source: 62.10032.061

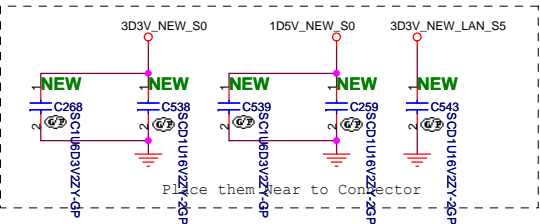


NEWCARD Connector

Reserve the symbol for bottom side connector



Place them Near to Chip



Place them Near to Connector

<Variant Name>

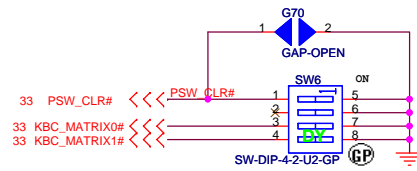
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI-PCI/NEW Card**

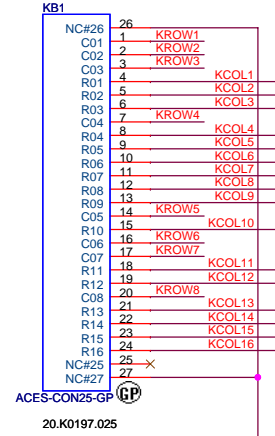
Size A3	Document Number	Rev SB
Garda5		

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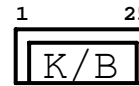
Internal Keyboard Connector



33 KROW[1..8] <<< ———
 33 KCOL[1..16] <<< ———



2nd source: 20.K0198.025

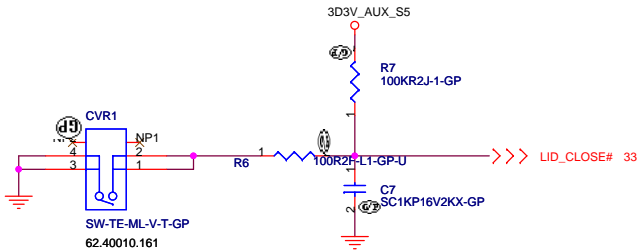


Keyboard matrix (from vendor)

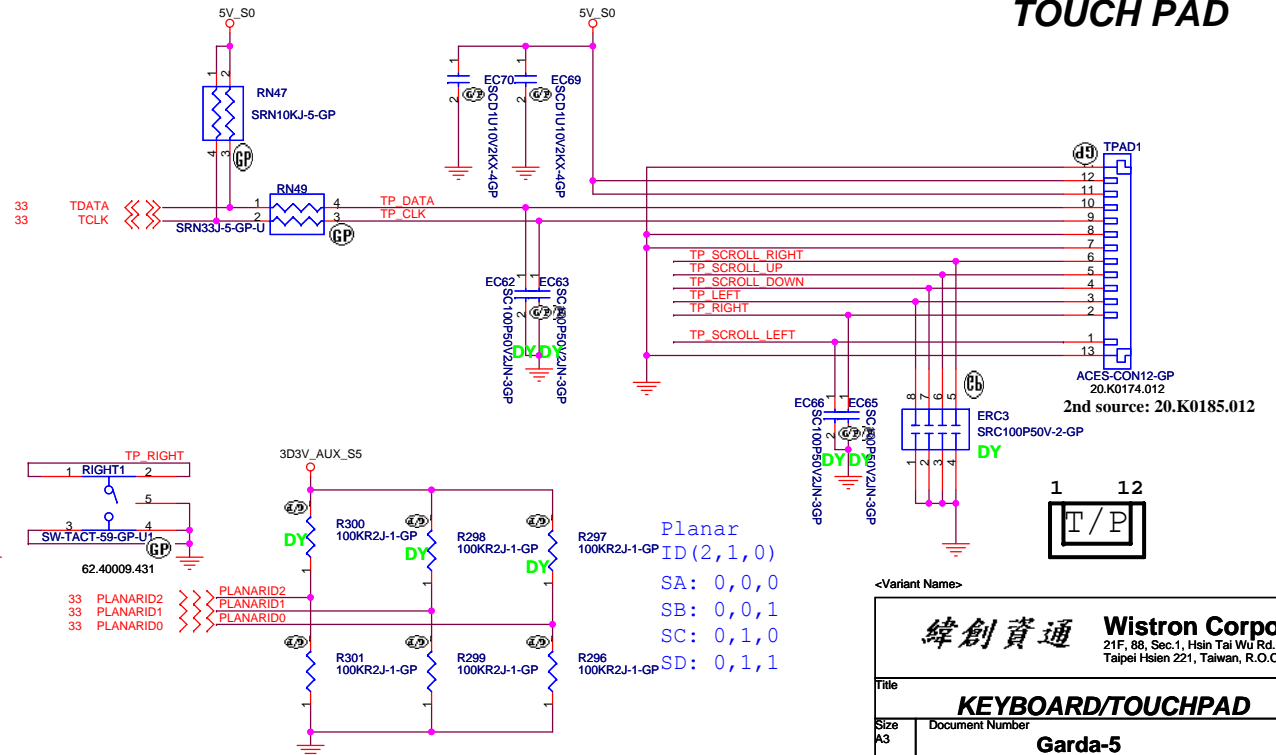
	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

	Low Active
PSW_CLR#	1 - 5 ON
NC	2 - 6 ON
RBC_MATRIX1	3 - 7 ON
RBC_MATRIX2	4 - 8 ON

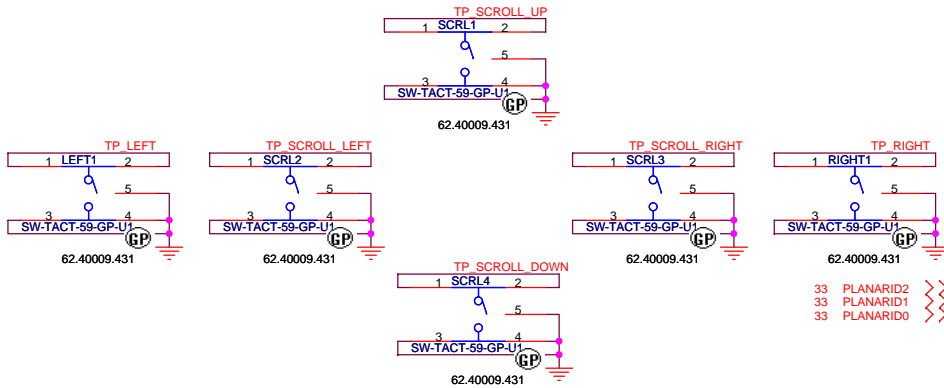
COVER SWITCH



TOUCH PAD

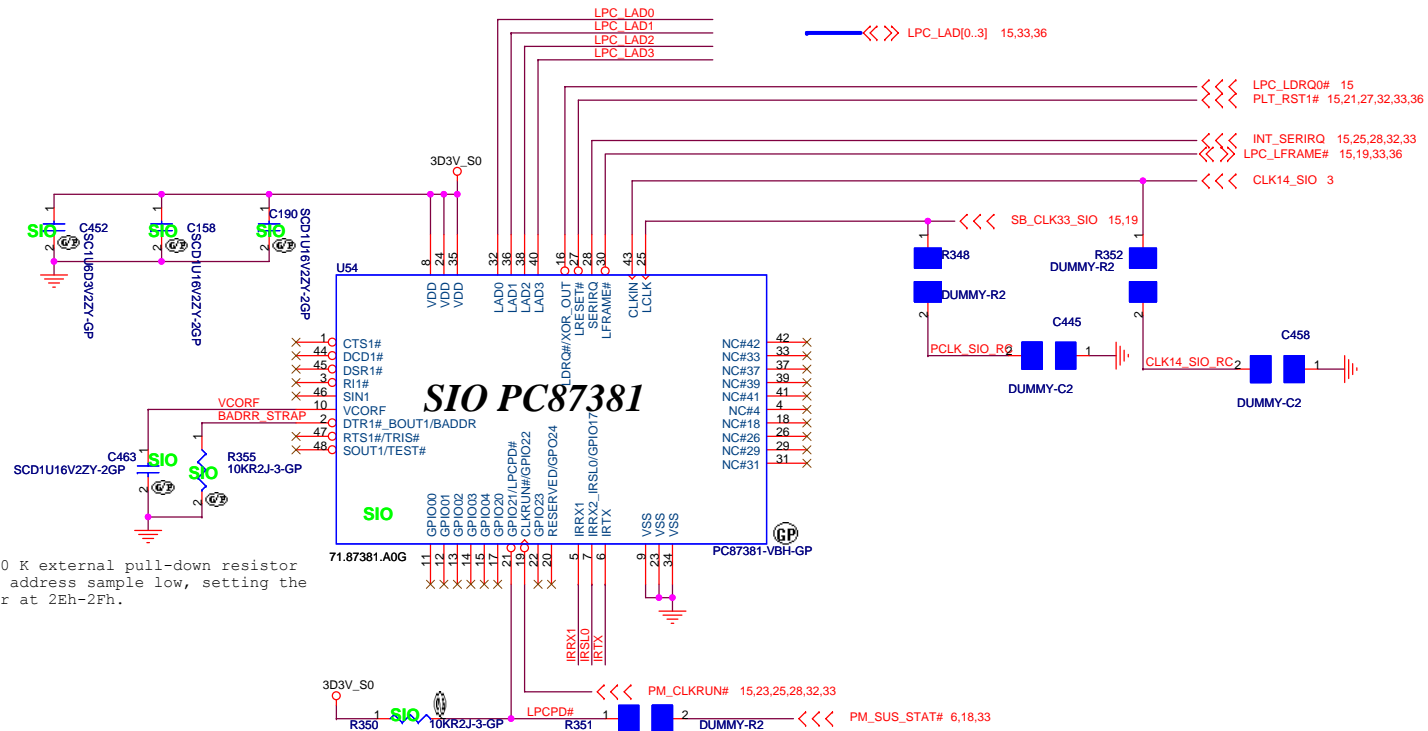


SCROLL KEY



緯創資通 Wistron Corporation
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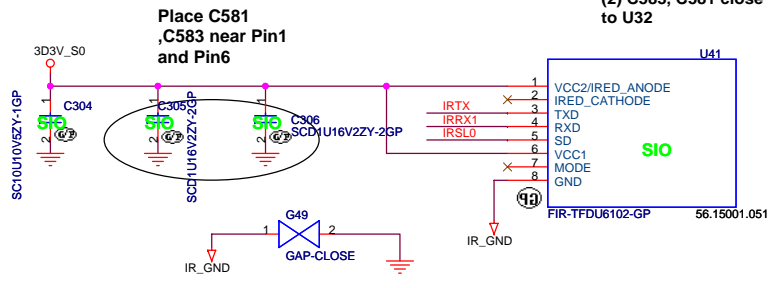
KEYBOARD/TOUCHPAD
 Title: KEYBOARD/TOUCHPAD
 Size A3 Document Number: Garda-5 Rev SA
 Date: Wednesday, April 26, 2006 Sheet 34 of 46



Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.

VISHAY FIR/CIR Module

- Layout Guide:
 (1) FIR_3D3V : 30 mils,
 (2) C583, C581 close to U32



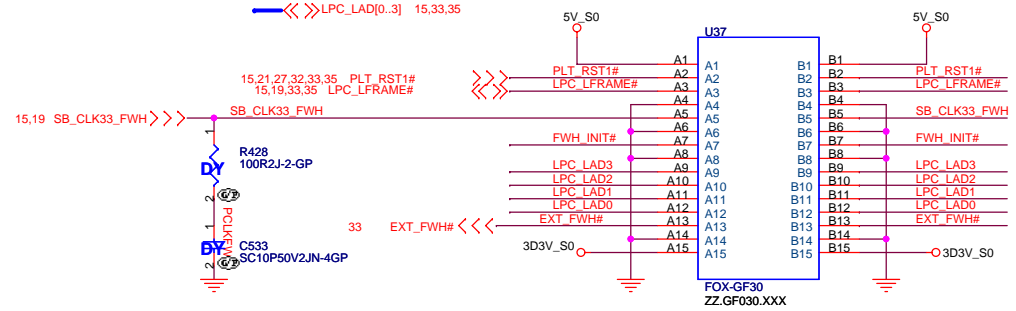
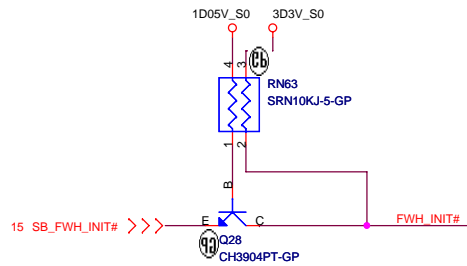
<Variant Name>

緯創資通 Wistron Corporation
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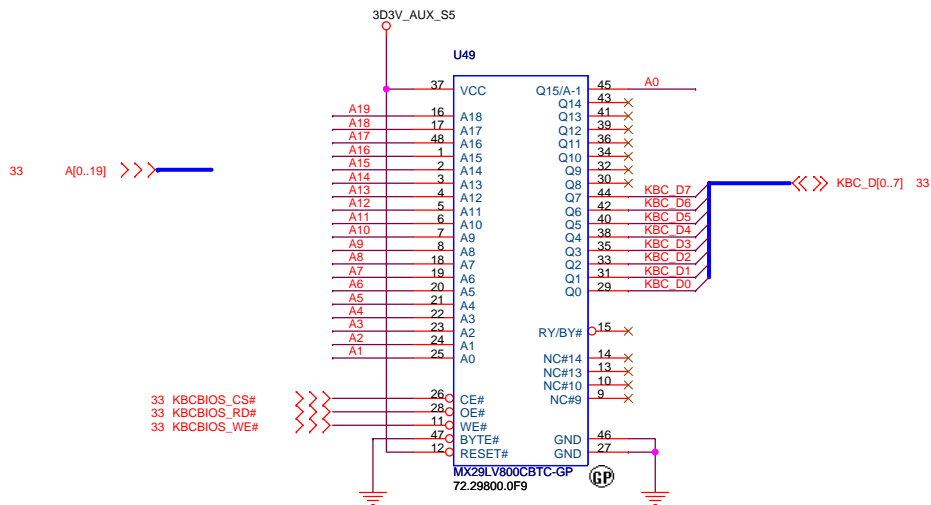
Title: **SIO 87381 / FIR**

Size A3 Document Number: **Garda-5** Rev: **SA**

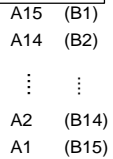
Date: Wednesday, April 26, 2006 Sheet 35 of 46



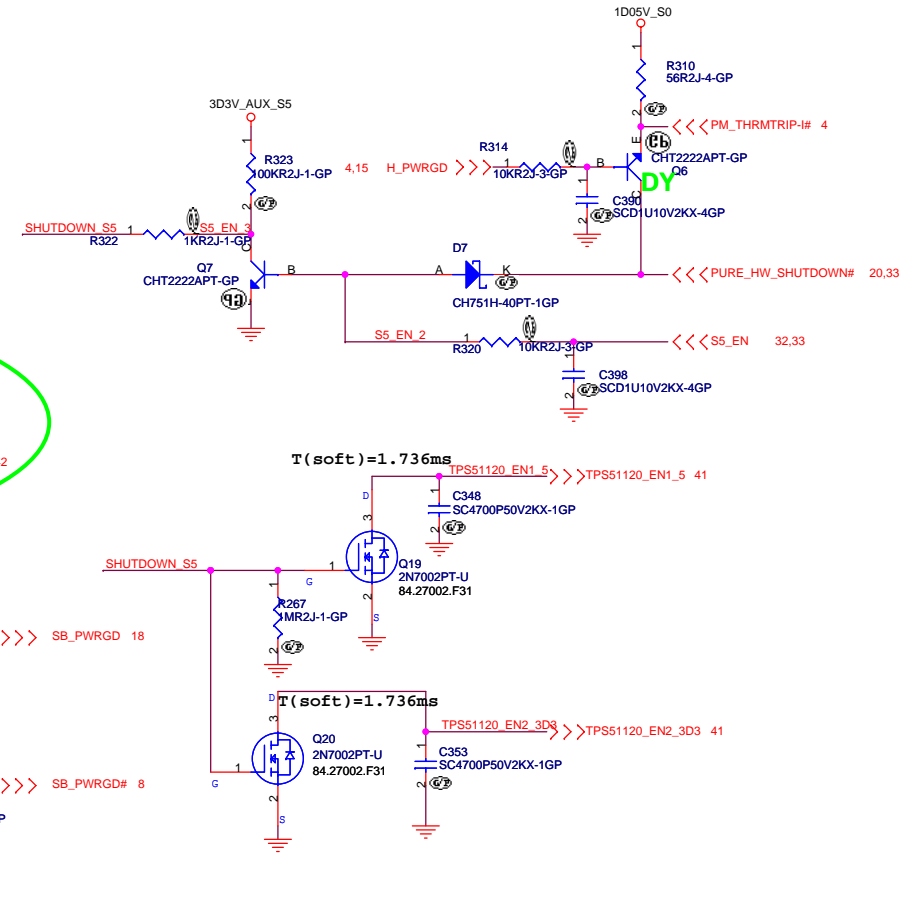
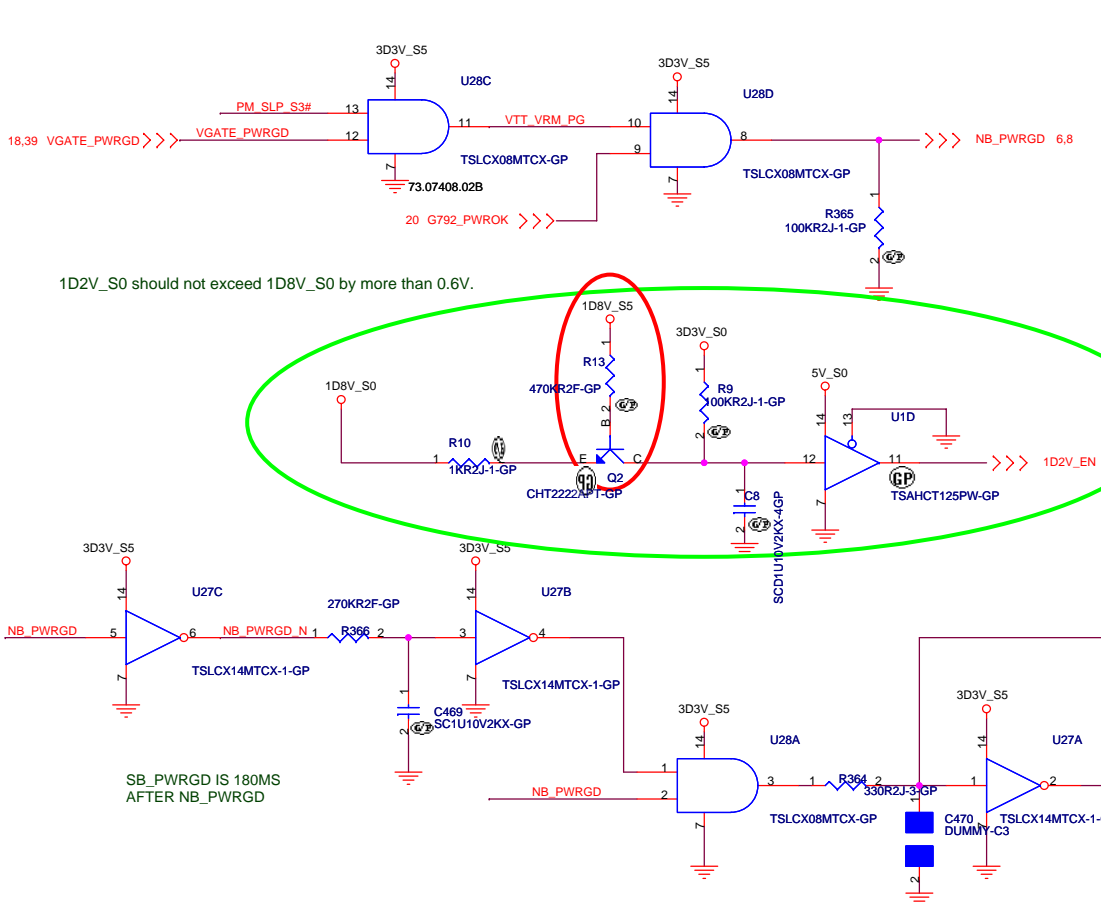
Boot Device must have ID[3:0] = 0000
 Has internal pull-down resistors
 All may be left floated
 FPET7 Elec. P3-46



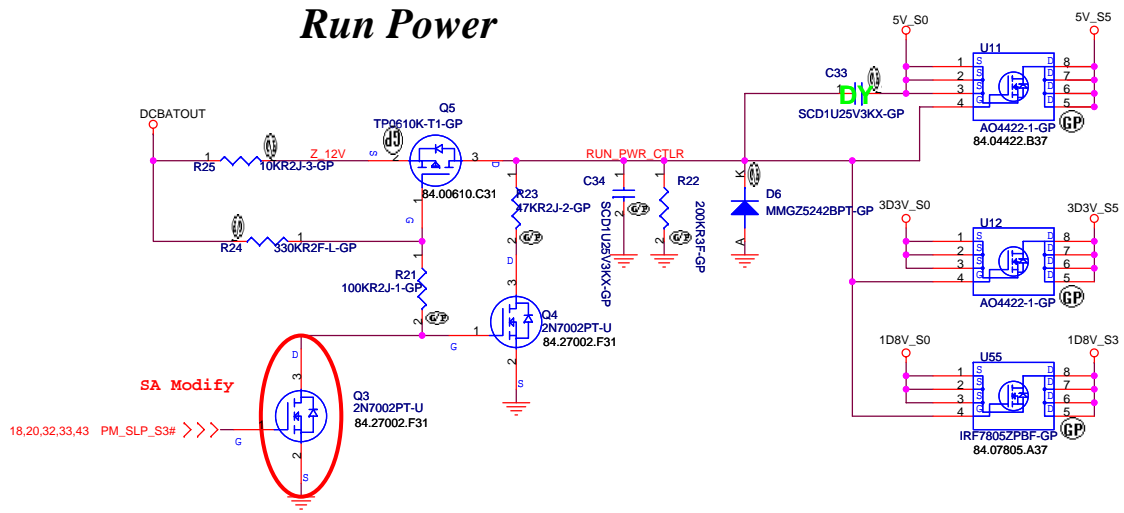
TOP VIEW



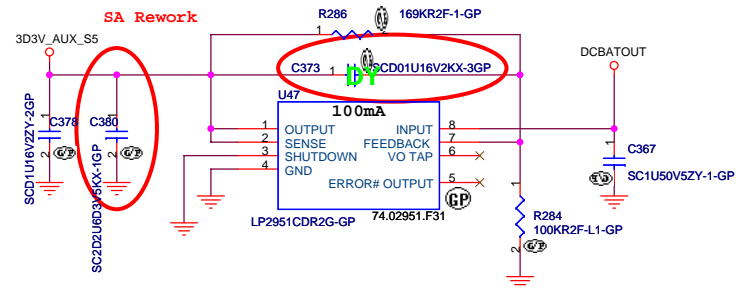
(BOTTOM VIEW)



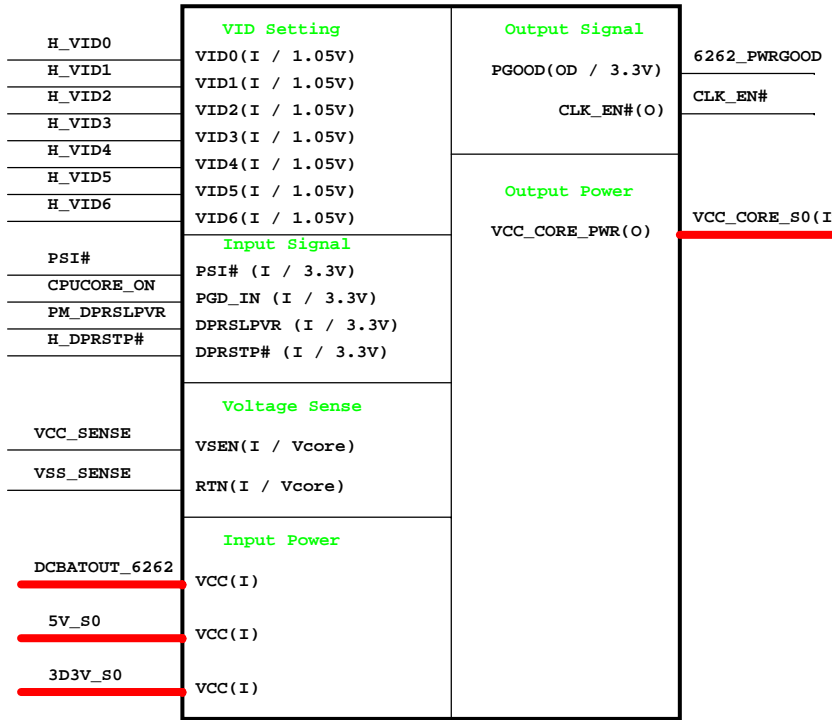
Run Power



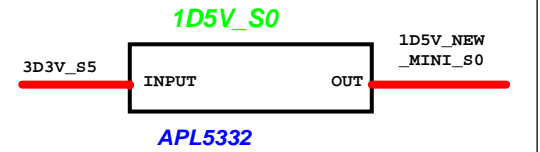
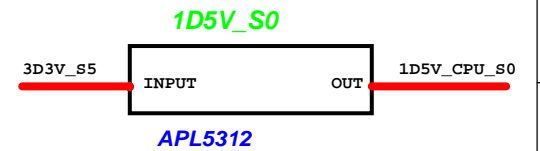
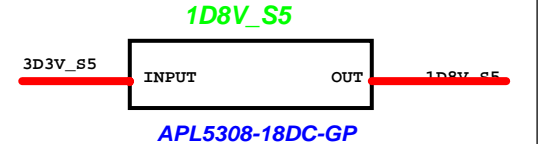
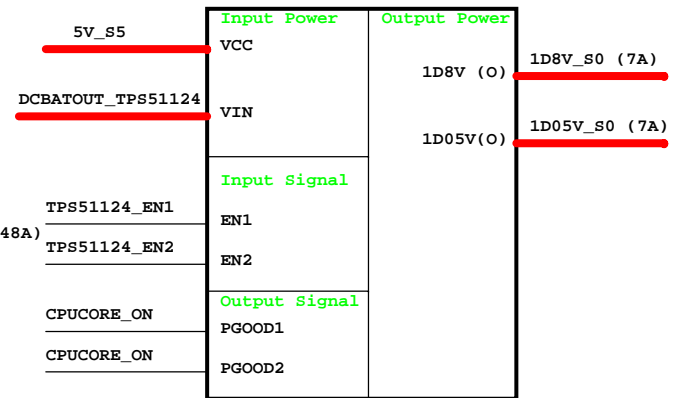
Aux Power



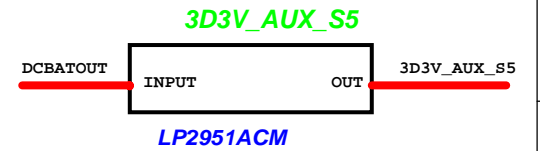
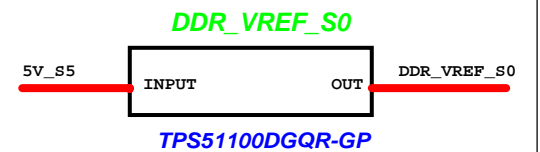
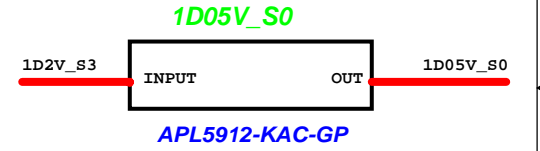
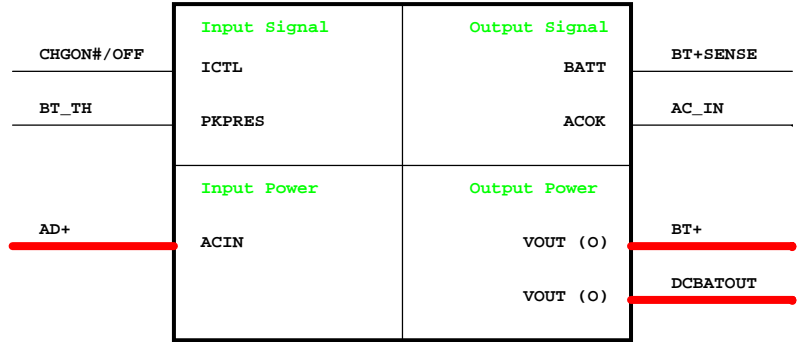
CPU_CORE
Intersil ISL6262



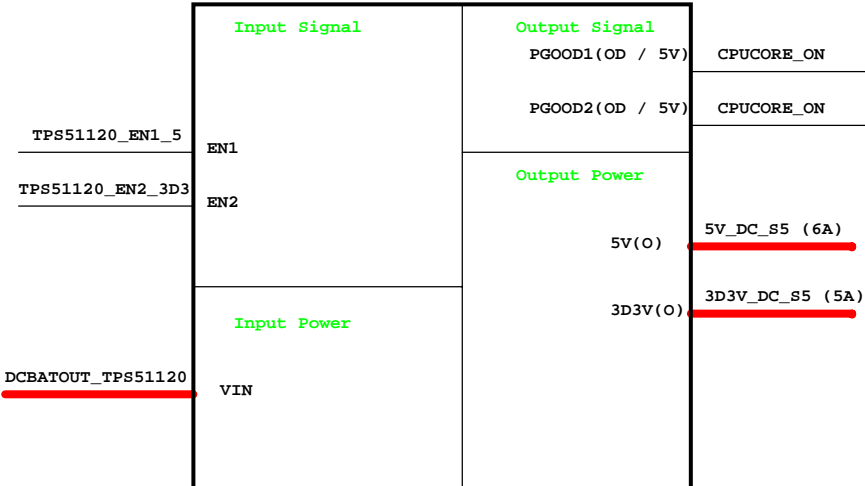
TPS51124
1D8V/1D05V



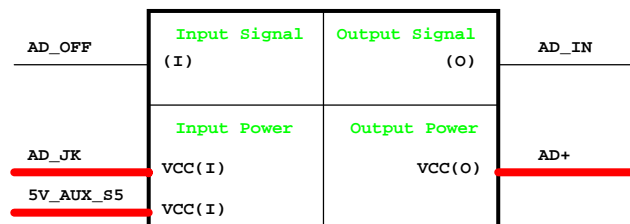
CHARGER MAX8725



TPS51120
5V/3D3V



Adapter



PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.

Place close to phase 1 choke
If NTC=330Kohm, R10=8.66K

SA Modify
Switching Frequency=300KHz

When test without cpu,
R183 & R184 change to 0 ohms
If VCC_SENSE and VSS_SENSE pins have pulled
resistors to VCC_CORE_S0
==> Remove R183/R184

Place close to phase 1 choke

Load Line

OCP >= 50A

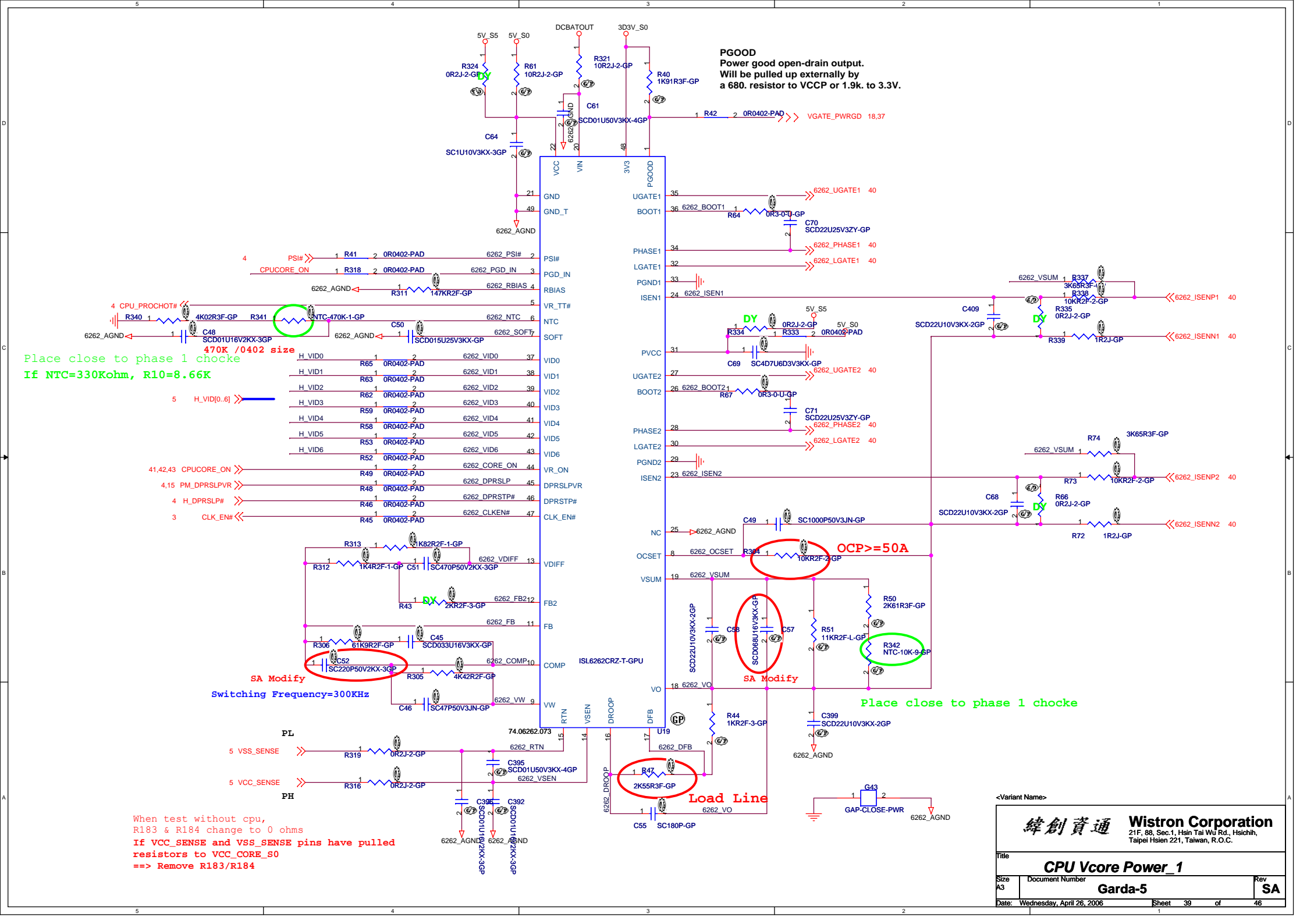
<Variant Name>

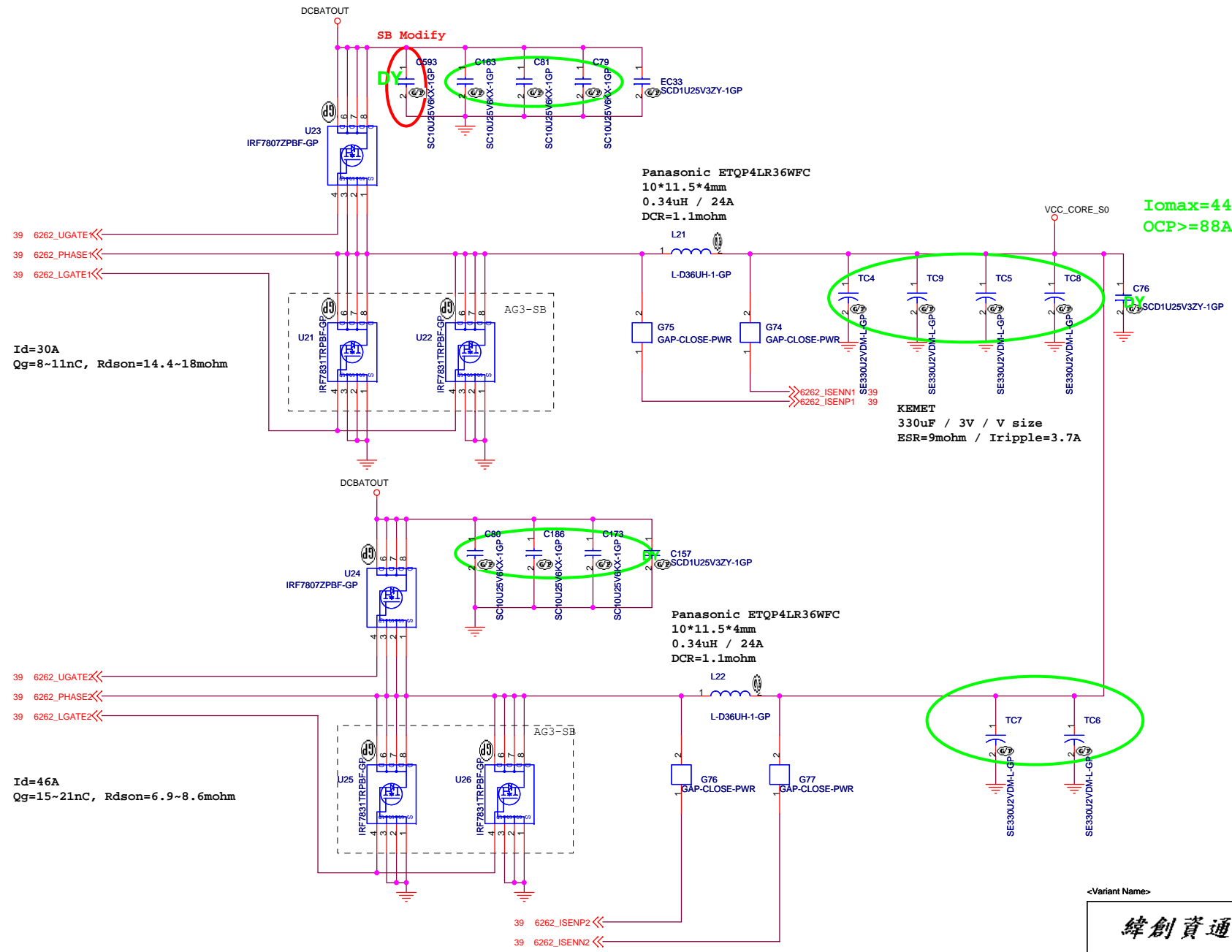
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU Vcore Power_1**

Size: A3 Document Number: **Garda-5** Rev: SA

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39 6262_UGATE<<
 39 6262_PHASE<<
 39 6262_LGATE1<<

Id=30A
 Qg=8-11nC, Rds(on)=14.4-18mohm

39 6262_UGATE<<
 39 6262_PHASE<<
 39 6262_LGATE2<<

Id=46A
 Qg=15-21nC, Rds(on)=6.9-8.6mohm

Panasonic ETQP4LR36WFC
 10*11.5*4mm
 0.34uH / 24A
 DCR=1.1mohm

KEMET
 330uF / 3V / V size
 ESR=9mohm / Iripple=3.7A

Iomax=44A
 OCP>=88A

39 6262_ISEN2<<
 39 6262_ISEN1<<

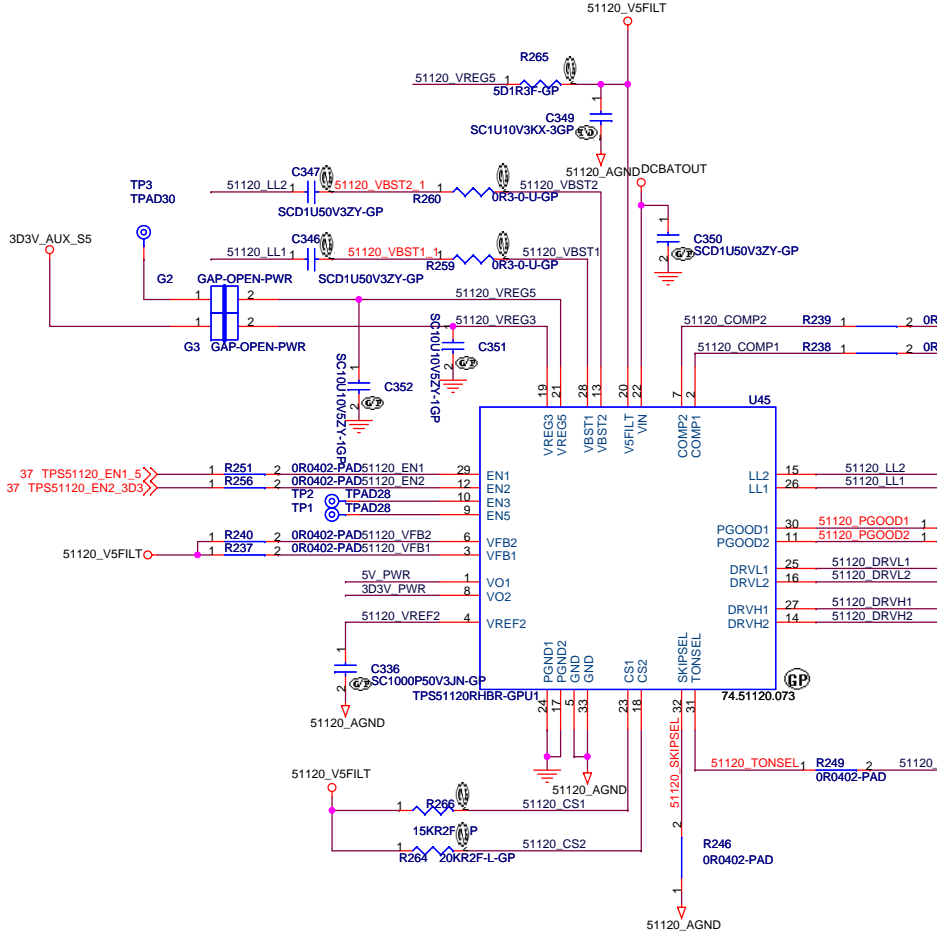
<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU Vcore Power_2/2

Size A3 Document Number **Garda-5** Rev **SB**

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Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

SB Modify

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

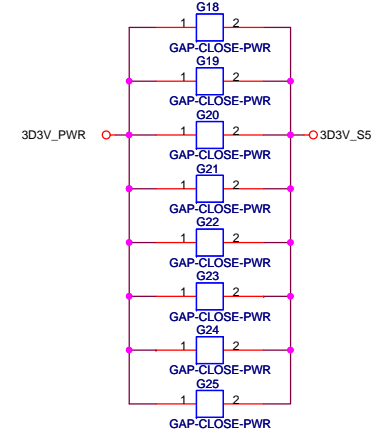
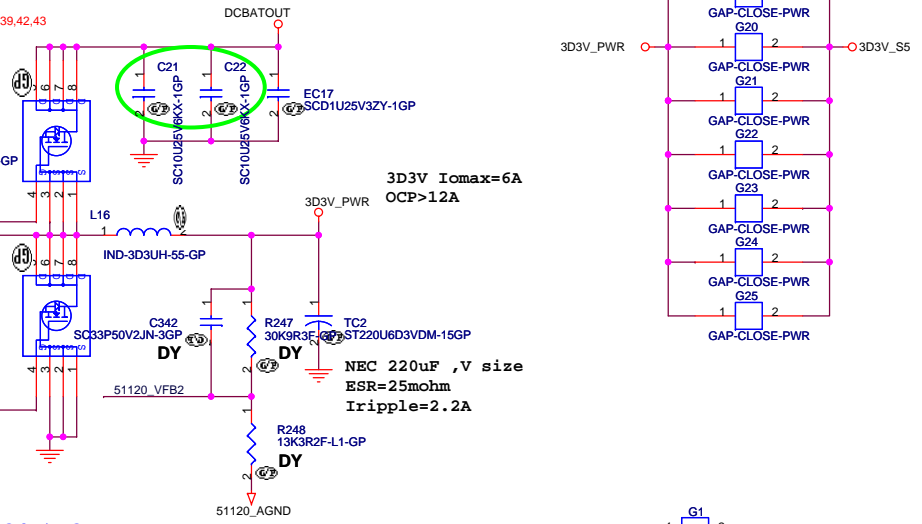
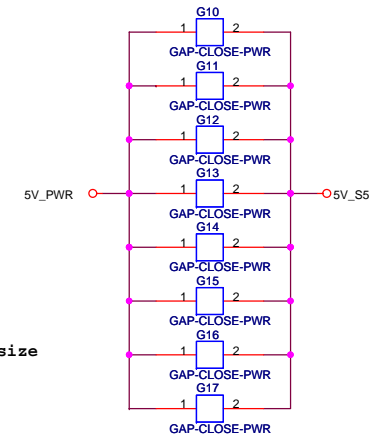
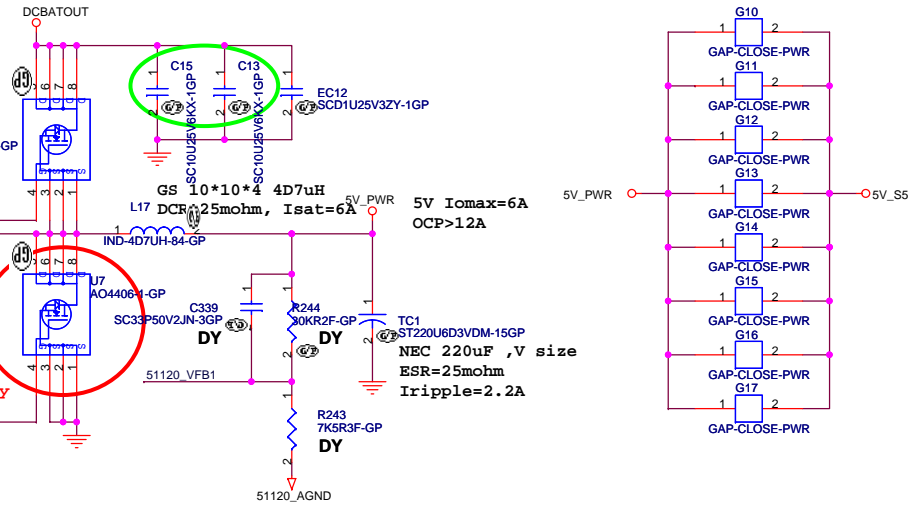
$$V_{out} = 1V * (R1 + R2) / R2$$

For TPS51120,
Vout=5V

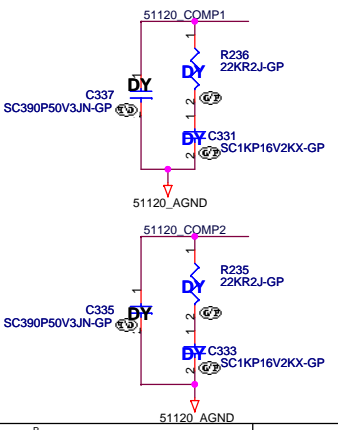
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Switchchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on



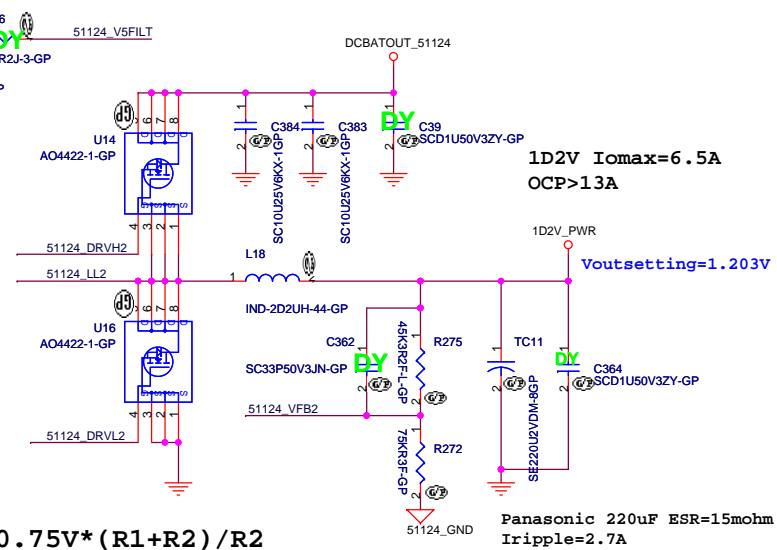
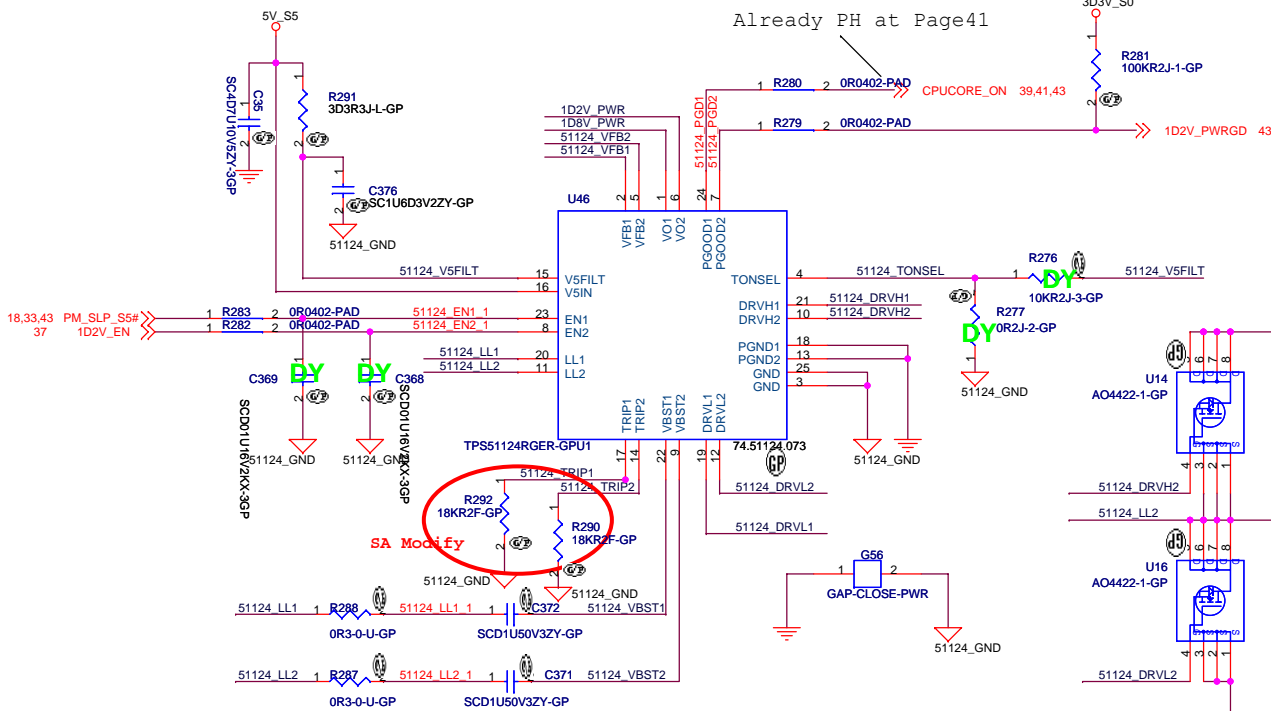
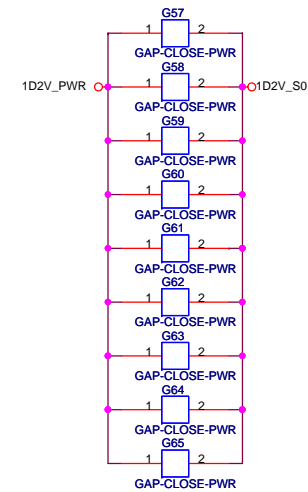
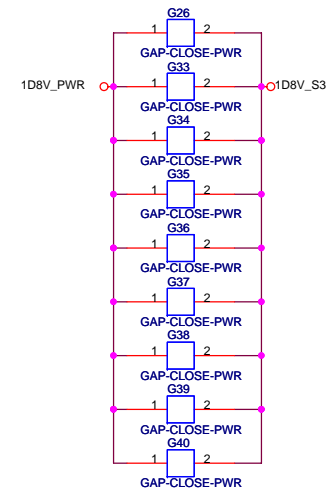
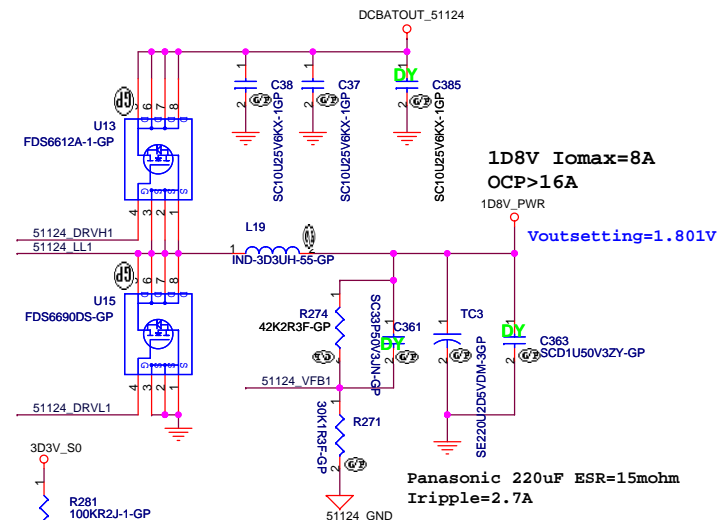
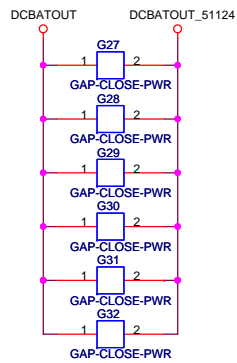
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51120_3D3V_5V**

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$$V_{out} = 0.75V * (R1 + R2) / R2$$

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

$$V_{trip}(mV) = R_{trip}(Kohm) * 10(\mu A)$$

$$I_{ocp} = (V_{trip} / R_{dson}) + ((1 / (2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$$

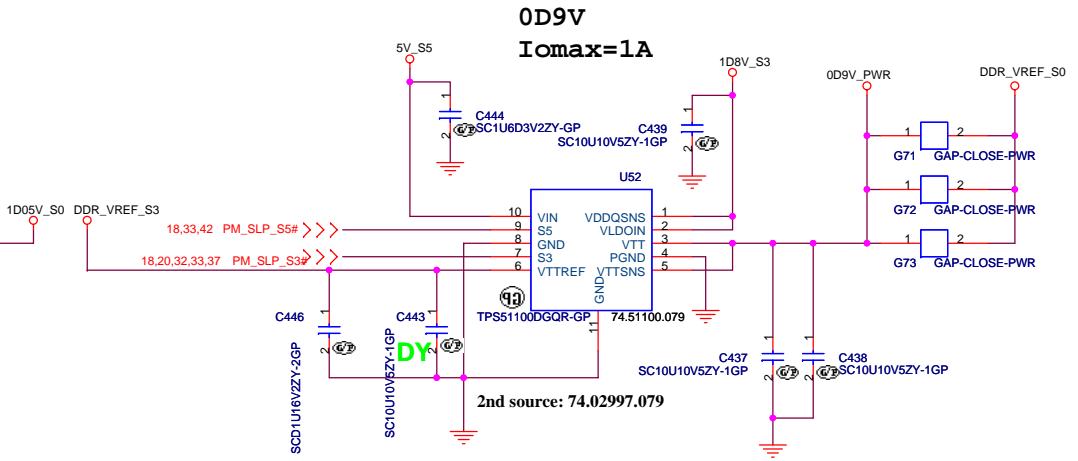
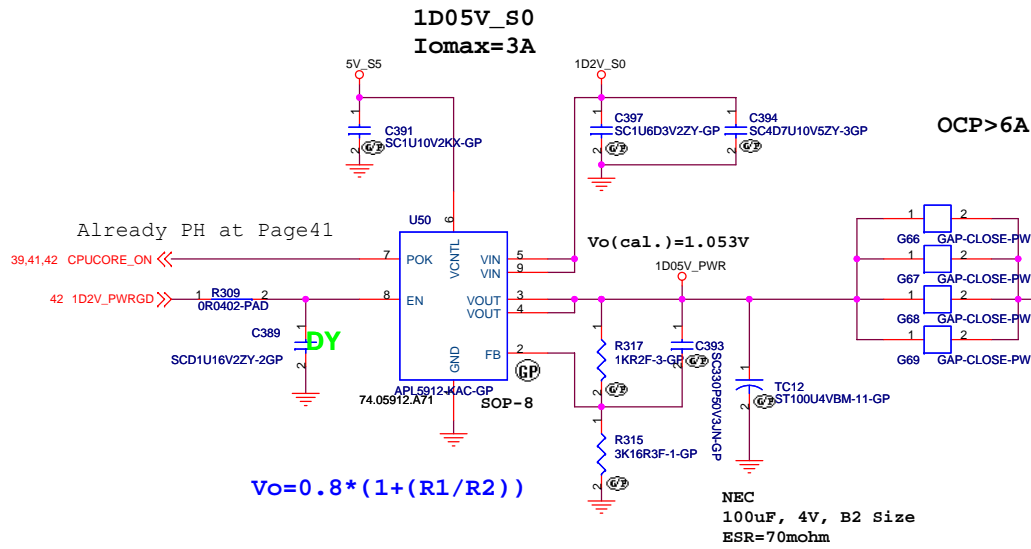
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

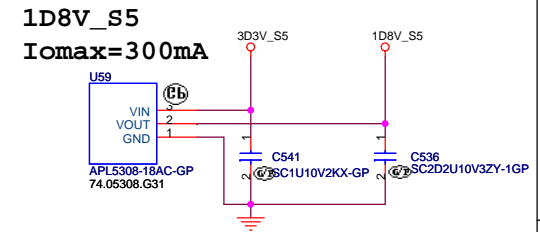
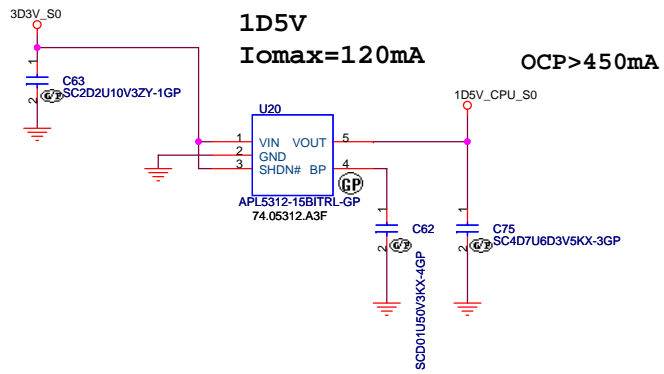
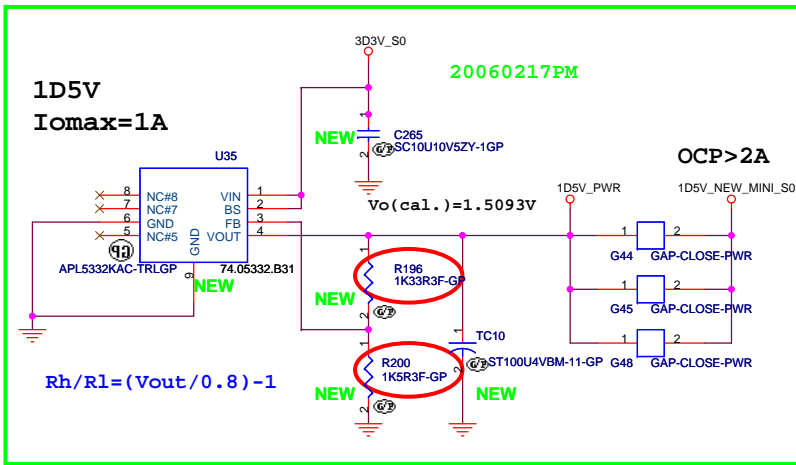
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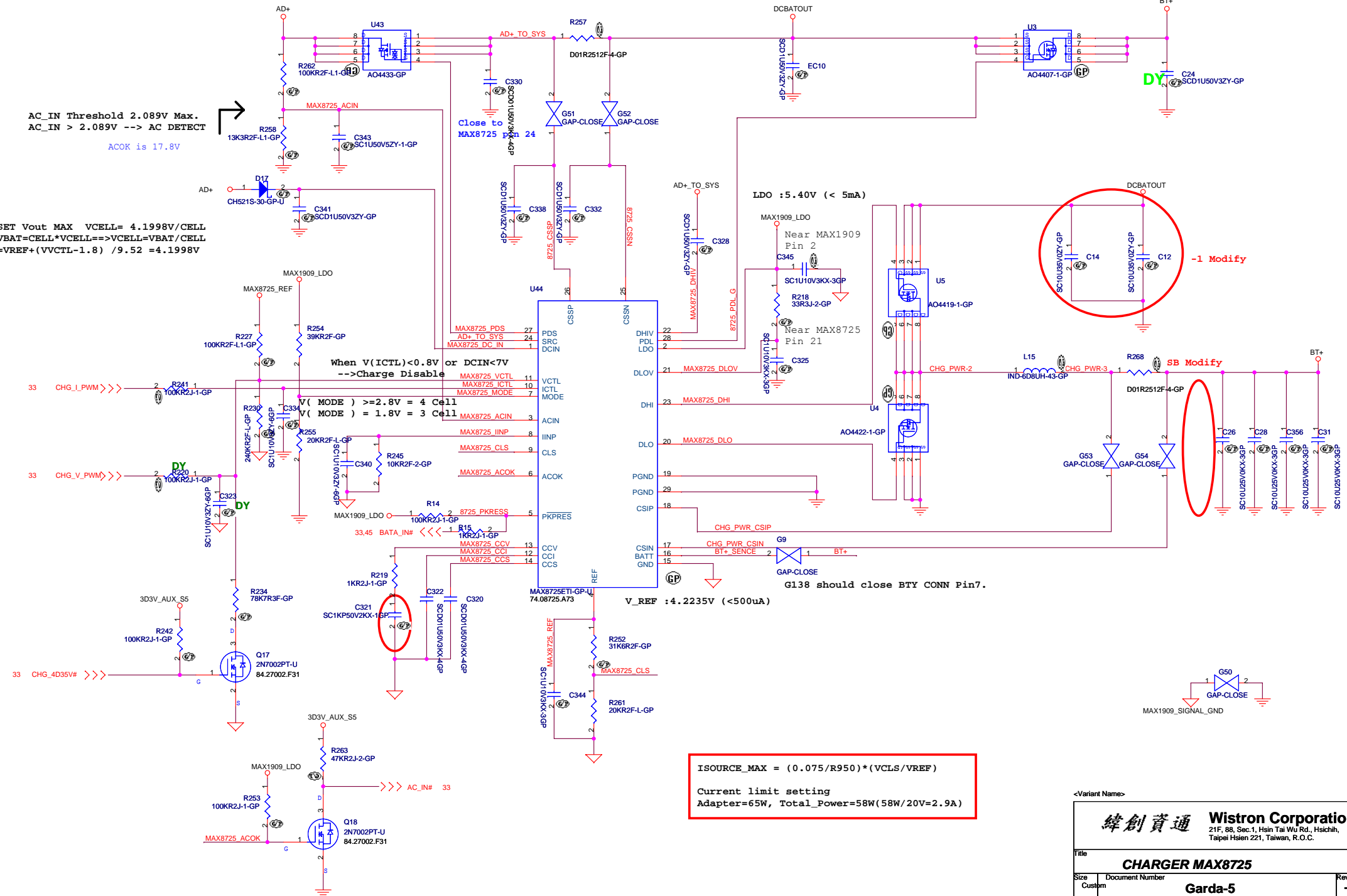


For New Card/MINI Card solution



AC_IN Threshold 2.089V Max.
 AC_IN > 2.089V --> AC DETECT
 ACOK is 17.8V

SET Vout MAX VCELL= 4.1998V/CELL
 VBAT=CELL*VCELL==>VCELL=VBAT/CELL
 =VREF+(VVCTL-1.8) / 9.52 =4.1998V



When V(ICTL)<0.8V or DCIN<7V
 -->Charge Disable

V(MODE) >= 2.8V = 4 Cell
 V(MODE) = 1.8V = 3 Cell

ISOURCE_MAX = (0.075/R950)*(VCLS/VREF)
 Current limit setting
 Adapter=65W, Total_Power=58W(58W/20V=2.9A)

<Variant Name>

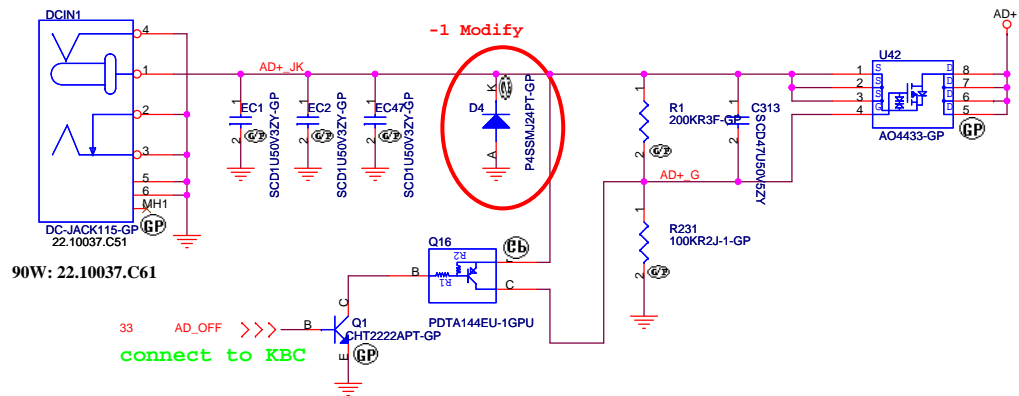
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER MAX8725**

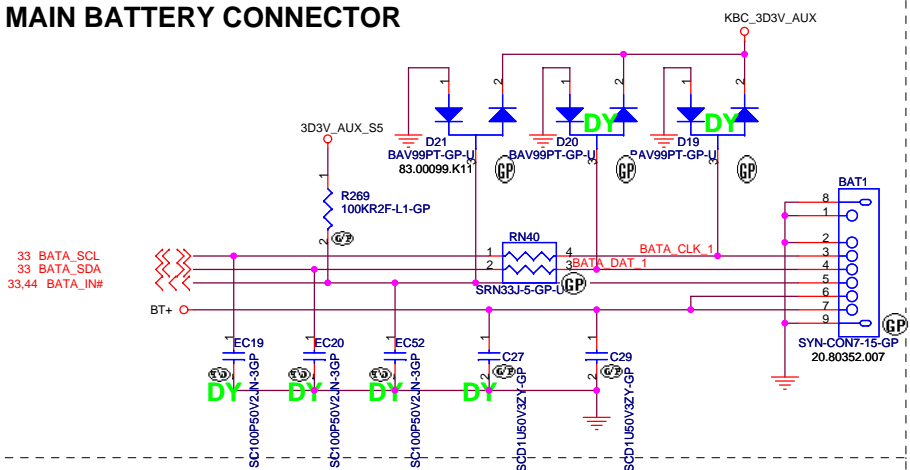
Size: Custom Document Number: **Garda-5** Rev: -1

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ADAPTER IN CIRCUIT



MAIN BATTERY CONNECTOR



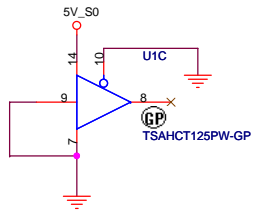
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

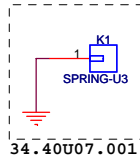
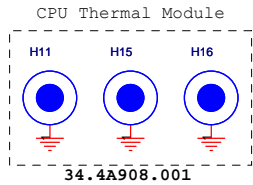
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Size: A3	Document Number: Garda-5	Rev: -1
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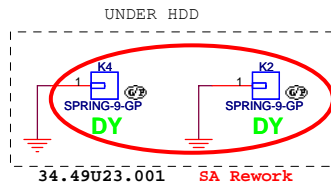
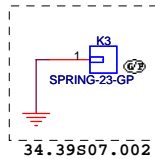
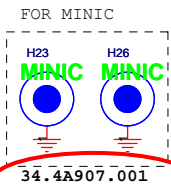
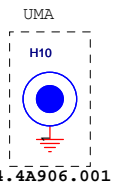
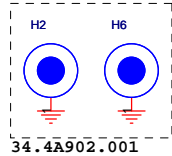
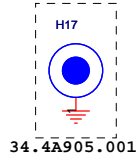
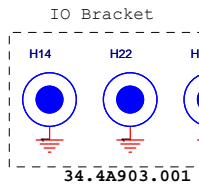
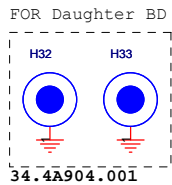
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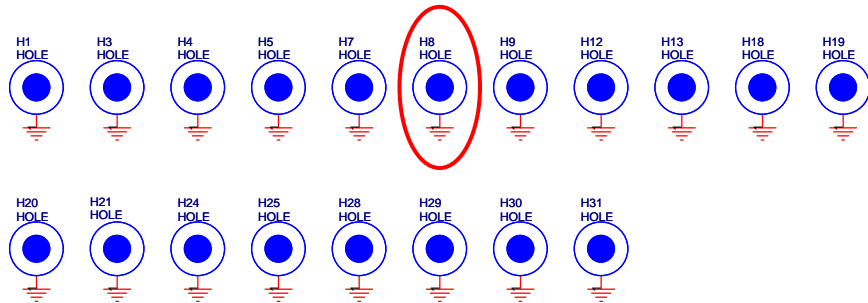
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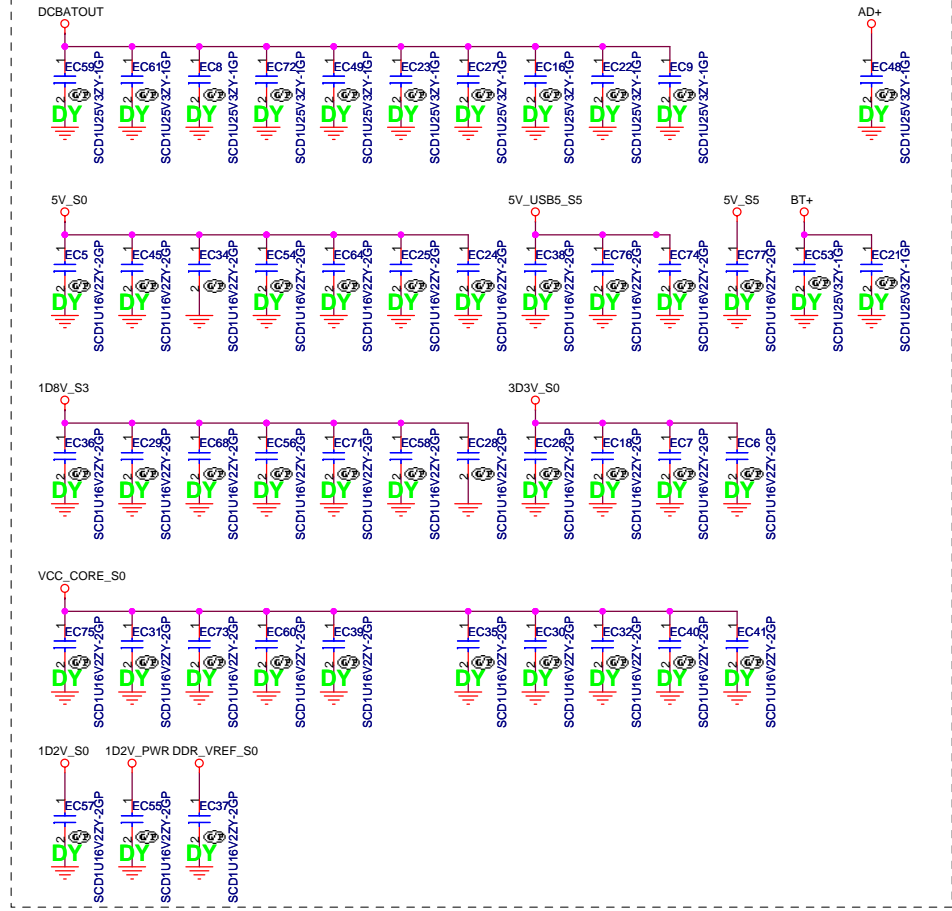
BOTTOM SIDE:



-1 Modify



EMI CAP



<Variant Name>

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SPRING & BOSS	
Garda-5	
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